Hardware Demonstration of Low-Rate and High-Dynamic Range ADC


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Motivation and Contributions

• Sampling and quantization are critical tasks of an ADC
• At high sampling rates ADCs are expensive and power consuming
• Large amplitude of the input compared to the dynamic range of an ADC results in clipped/saturated signal during quantization
• To address clipping, modulo (wrapping) operation is applied on the signal to restrict the dynamic range
• Existing reconstruction algorithms operate at a much higher rate compared to the rate without a modulo operation
• We propose a new $B^2R^2$, Beyond Bandwidth Residual Recovery, algorithm so that unwrapping can be performed robustly at a low sampling rate
• We propose a dedicated hardware prototype that can handle high frequency and high amplitude input signal

Dynamic Range of ADC

• The ratio of maximum amplitude of an input and the dynamic range of an ADC is crucial in signal processing

Modulo Sampling and Reconstruction

• To avoid clipping, an unlimited sampling approach (based on Higher Order Difference-CPF) is proposed by Bhandari et al. IEEE TSP 2020 and Chebyshev Polynomial Filtering (CPF) approach is proposed by Ordentlich et al. IEEE SPL 2019
• To restrict the amplitude of the input, $f(\theta)$, within the dynamic range, $\lambda$, the above approaches uses a modulo operation, $M(\lambda)$
• HOD: The reconstruction algorithm, $R$, operates at 17 times the Nyquist and is not robust to noise
• CPF: The reconstruction algorithm, $R$, is not robust to noise
• We demonstrate an alternative algorithm called $B^2R^2$ that operates at 3 times the Nyquist rate in the presence of noise

$B^2R^2$ Algorithm


Aim: Estimation of $z[n]$ using the two properties of given finite energy bandlimited (BL) signal

Property 1: Time-Domain separation

\[ \exists N_2 \in \mathbb{N}: z[n] = 0, \forall |n| > N_2 \]

Property 2: Fourier-Domain separation

\[ \mathcal{F}_2(z[n]) = \mathcal{F}_3(f_3[n]) \quad r = (\pm \pi, \pm \rho \pi) \]

Formulating Convex Optimization Problem:

\[ \min \| \mathcal{F}_2(f_3 - o) \|_2 \quad s.t. \quad z[n] = 0, \forall |n| > N_2 \]

Hardware

Subtractor

Comparators

Multiplier

Bit DAC

Signal Generator (Microcontroller)

Modulo Board

Graphical User Interface

User Interface

Low and High-Dynamic Range ADC

Simulation Results

$B^2R^2$ is robust to noise

Hardware Results

Nyquist: 20kHz; HOD: CPF; $B^2R^2$: 6kHz

SNR: 20dB

Sampling rates: Nyquist 20kHz, HOD: 34kHz; Proposed approach: 6kHz

Results

Modulo Board Details

• Board characteristics:
  - Has the ability to handle input amplitude that is 8 times the dynamic range
  - Provides high frequency support
• The folding is done with: (a) Comparators – in order to identify the input signal level, (b) 3 Bit DAC, (c) Multiplier and (d) Subtractor in order to adjust the analog signal prior to sample it via a standard ADC

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