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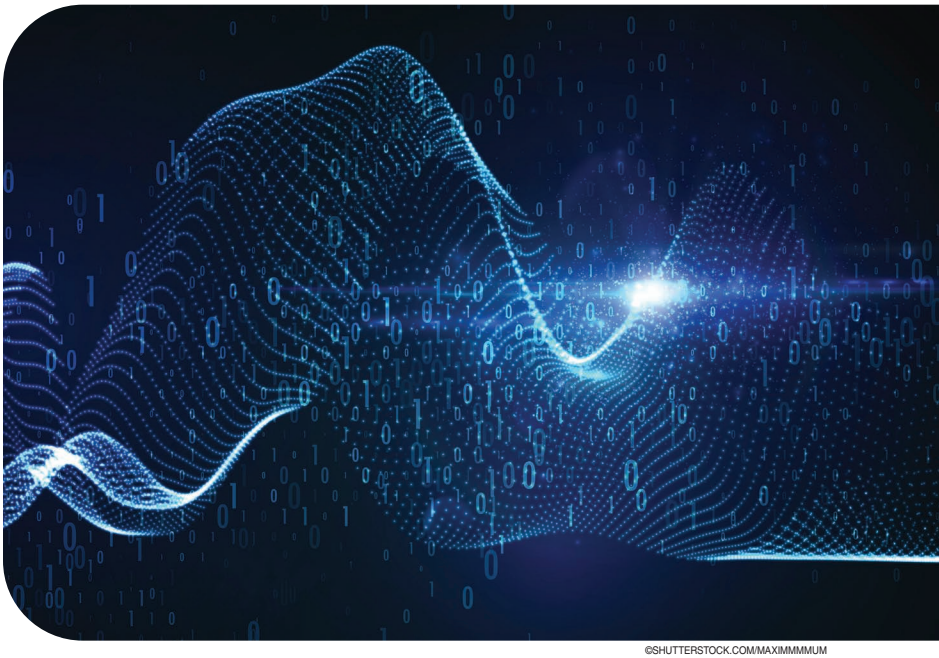
Power-Efficient Sampling

Towards low-power analog-to-digital converters

Analog-to-digital converters (ADCs) facilitate the conversion of analog signals into a digital format. While the specific designs and settings of ADCs can vary depending on the application, it is crucial in many modern applications to minimize the devices' power consumption. The significance of low-power ADCs is particularly evident in fields like mobile and handheld devices reliant on battery operation. Key parameters that dictate ADCs' power are the sampling rate, dynamic range (DR), and number of quantization bits. Typically, these parameters are required to be higher than a threshold value but can be reduced by using the structure of the signal and by leveraging preprocessing and the system application needs. In this article, we discuss four approaches relevant to a variety of applications.



Introduction

Real-world signals, including speech, audio, biomedical data, radar readings, communication transmissions, and more, inherently exist in an analog format. Transforming these signals into a digital representation is often a more efficient way to process, compress, store, and transmit them when considering factors like power efficiency, noise resistance, and algorithms' adaptability. Therefore, the digital conversion of analog signals is central to any application involving real-world signals.

To achieve this digital representation, ADCs are employed. Given that ADCs are an essential component in many applications, their design and selection of parameters, such as the sampling rate, the number of bits for quantization, and the DR, are critical factors in effectively addressing the requirements of a particular application. For instance, when it comes to accurately reconstructing band-limited signals from uniformly spaced samples, the ADC's sampling rate should meet or exceed the Nyquist rate, which is twice the maximum frequency component of the analog signal. In a similar vein, the DR of the ADC should exceed that of the signal to prevent signal clipping during the sampling process, and a greater number of bits results in reduced quantization errors.

In emerging fields like wearable biosensors, wireless sensor networks, voice-activated interfaces (such as Amazon's Alexa, Apple's Siri, Microsoft's Cortana, and Google's Assistant), Internet of Things sensors, and more, the power consumption of ADCs holds great importance. Take, for example, wearable biosensors, which can monitor parameters like blood pressure, electrocardiogram readings, and epilepsy seizures. These devices often operate within

D. Van De Ville acted as the associate editor for this article and recommended it for publication.

Digital Object Identifier 10.1109/MSP.2025.3543669
Date of current version: 17 July 2025

stringent resource limitations, including power and space constraints, especially since many of them rely on battery power with finite energy reserves. In such applications, efficiently reducing power requirements for the sensor's ADCs is essential to ensure uninterrupted monitoring of the signals. Likewise, in any voice-activated interface, the voice detection sensors remain active continuously, underscoring the significance of minimizing the power demands of their ADCs. Furthermore, in applications that deal with wideband signals, the power consumption of the ADC is notably high due to the need for a high sampling rate, and this element constitutes a significant portion of the overall power requirements of the system.

In this article, we explore signal processing-based techniques and frameworks to lower the ADC power and the entire system power. A common theme is to enable analog preprocessing prior to sampling together with postprocessing on the signal in order to reduce the ADC power while still enabling signal recovery. The recovery may involve either reconstructing the original analog signals from the collected samples or estimating certain parameters. The power consumption of a conventional ADC, which captures uniformly spaced instantaneous samples of the analog signal, increases in tandem with the sampling rate, the number of bits used, and the DR of the ADC. To address this challenge, we delve into theoretical lower limits on the power consumption of ADCs [1] and also examine a few figures of merit (FOMs) employed for assessing commercially available ADCs [1], [2]. Once these relationships are established, various frameworks can be applied to mitigate the impact of these factors on power requirements.

We consider the following four approaches for power reduction: 1) sub-Nyquist sampling, where the signal's structure is used to reduce the sampling rate [3]; 2) the modulo ADC, where a low-DR ADC preceded by a folding circuit is used to sample high-DR signals without clipping [4], [5], [6]; 3) event-based sampling, where time instants at which a signal crosses a set of thresholds are used as the discrete representation [7], [8], [9], [10]; and 4) low-bit quantization methods, in which the number of bits is reduced when the end task is to recover a few parameters of the signal [11], [12].

The majority of these frameworks comprise three primary components: 1) analog preprocessing hardware or an analog front end, 2) a traditional low-power ADC, and 3) a digital processing module. The preprocessing component alters the analog signal in a manner that allows the ADC to function at a reduced sampling rate, a lower bit rate, or a narrower DR compared to an ADC lacking preprocessing. The digital processing segment encompasses algorithms that can potentially reverse the impact of the preprocessing stage and includes reconstruction or recovery algorithms. We detail these components' integrated design, considering theoretical and practical perspectives. In the theoretical realm, we present assurances for achieving perfect signal recovery and examine algorithms concerning critical parameters like the sampling rate, number of bits, and DR. Subsequently, we explore the influence of these parameters on power consumption and hardware design. In addition, we also discuss existing hardware prototypes for these various approaches [13], [14], [15], [16], [17], [18], [19], [20].

In the following section, we discuss bounds and FOMs, which will be used to assess the power saving aspects of the considered frameworks.

Power consumption of an ADC and FOMs

We first discuss the bounds of the power consumption of a conventional ADC, which are used throughout the article to compare different ADCs. The flash ADC topology is selected to represent a conventional data converter, due to its wide usage and simplicity in estimating power consumption across various ADC parameters (resolution, sampling frequency, and others). The details are given in "Power Consumption of the Conventional Flash Analog-to-Digital Converter." We refer the readers to [1] and the references therein for details of these derivations.

From (S3), we infer that the power consumption increases linearly with the sampling rate and exponentially with the number of bits. These observations are based on theoretical analysis, and in practice, the power dependency on the sampling rate and number of bits could be different. To understand the practical aspect, we consider the surveys considered in [2] and a recent one by Murmann [21]. These reports compare various ADCs in terms of different FOMs. As an example, Walden's FOM for a conventional ADC is given as [2]

$$\mathrm{FOM}_W = \frac{P}{2^{\mathrm{ENOB}} f_s} \tag{1}$$

where P is the power consumption of the ADC, f_s is the sampling rate, and ENOB is the effective number of bits. An empirical study of the available ADCs in [21] shows that the FOM_W does not change as f_s changes for $f_s \leq 100$ MHz. MHz. This implies that P is proportional to f_s. However, for $f_s > 100$ MHz, the behavior of FOM_W as a function of f_s reveals that the increase in power consumption due to the sampling frequency exceeds the linear increment, which means that the actual power saving of sub-Nyquist is more than the theoretical power saving. Further, the reviews reveal that in commercially available ADCs, the sampling rate and number of bits are typically not independent. Specifically, the number of bits decreases with an increased sampling rate, owing to design constraints.

In the aforementioned analysis, we do not observe an explicit dependency of the power consumption on the DR. Rather, the power consumption is an implicit function of the DR, as shown next. Consider two ADCs with DRs $[-\lambda_1, \lambda_1]$ and $[-\lambda_2, \lambda_2]$, respectively, where $\lambda_1 > \lambda_2$. Let the resolutions of the two ADCs be N_1 and N_2 bits, respectively. Then, the quantization noise powers are given as $(1/12)(\lambda_1/2^{N_1-1})^2$ and $(1/12)(\lambda_2/2^{N_2-1})^2$. To keep the same quantization error for both ADCs, the number of bits should satisfy the equality $N_1 = N_2 + (\lambda_1/\lambda_2)\log 2$. Hence, for a high-DR ADC, one must choose a larger number of bits to keep the

same quantization error level. Following (S3), this results in higher power consumption.

In summary, the power consumption of an ADC increases with the sampling rate, number of bits, and DR. In the following, we discuss how to reduce these quantities and, eventually, the power consumption without compromising the quality of the reconstruction or task. In general, these quantities are reduced by analog preprocessing steps, which could consist of either single-channel or multiple-channel front-end circuits. These front ends could be realized using off-the-shelf components or custom-designed analog and radio-frequency circuits with low power consumption by codesigning digital signal processing (DSP) and analog preprocessing. Hence, the overall power consumption of the circuit can be made lower than the corresponding conventional circuit.

Sub-Nyquist sampling

In most practical applications, analog signals are either assumed to be band limited or maximally band limited. In the latter case, one assumes that most (e.g., 99%) of the signal's energy lies in a frequency range known as the signal's *effective bandwidth*. These signals are sampled according to the well-known Shannon–Nyquist sampling framework [3]. In this framework, the signals are first passed through an antialiasing filter to project the signals to a band-limited space and then sampled uniformly at the Nyquist rate, which is twice the maximum frequency content of the signals. Since the power consumption of ADCs increases with the sampling rate, the Shannon–Nyquist framework leads to higher power consumption for wideband applications, such as ultrawideband radar, cognitive radio, and wideband communications, where the bandwidth of the signals is on the order of gigahertz.

A solution to this problem is to explore signal structures beyond band limitedness and reduce the sampling rate below the Nyquist rate (sub-Nyquist sampling) by using the signal structure or model. Many signals encountered in practice have sparse representations either in the time or frequency domains, which leads to sub-Nyquist sampling. Several review articles on sub-Nyquist sampling exist from both theoretical aspects [3], [15], [22] and practical considerations [20], [23]. Hence, in this article, we keep the discussion of the sub-Nyquist theory short and focus on the power savings that can be obtained through this approach. In particular, we consider two signal models, finite-rate-of-innovation (FRI) signals [24], [25], [26], [27] and multiband signals [14], [28], [29], [30], and discuss their power efficiency aspects.

FRI signals

In many applications, the signals can be specified by a finite number of parameters per unit time interval. As the rate of

Power Consumption of the Conventional Flash Analog-to-Digital Converter

To facilitate a more detailed discussion on power-efficient sampling techniques, we consider two major components of a flash analog-to-digital converter (ADC), a widely used high-speed architecture: 1) the sample-and-hold (S/H) circuit, which includes a switch and a sampling capacitor that samples and retains the analog signal value for subsequent quantization, and 2) the quantizer, which utilizes analog comparators to convert the sampled value from the S/H circuit into a corresponding bit stream (See Figure S1). The total power consumption is the sum of the S/H circuit and the comparators. To derive the total power, we assume that the capacitors used in the S/H and quantizers are chosen to be large enough such that the thermal noise is less than or equal to the quantization error [1]. For deriving the quantization error, we assume that the input signal $f(t)$ lies in the amplitude range $[-A, A]$ and that the quantizer has n bits. With these assumptions, the power consumption in the S/H is given as

$$P_S = 24kTf_s 2^{2n} \tag{S1}$$

where k is Boltzmann's constant and T is the absolute temperature in degrees Kelvin. In the quantizer part, an expression for power consumption in each comparator is derived as

$$P_C = 4n \ln 2 V_{\text{eff}} C_C f_s A \tag{S2}$$

where C_C is the load capacitance of the latch comparator. The quantity V_{eff} is a parameter of the comparator and is defined as $V_{\text{eff}} = g_m I_D$, where I_D is the supply current of the comparator and g_m is the minimum transconductance of the comparator to make a decision within the sampling period. Hence, the total power of a conventional flash ADC is

$$P = P_S + (2^n - 1)P_C = 24kTf_s 2^{2n} + 4(2^n - 1)n \ln 2 V_{\text{eff}} C_C f_s A. \tag{S3}$$

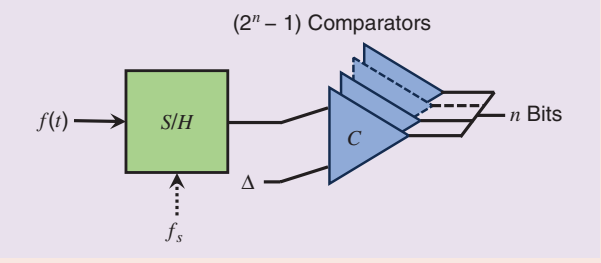


FIGURE S1. A conventional flash-type ADC with an S/H circuit operating at a sampling rate f_s and a quantizer consisting of 2^n comparators, where n is the number of bits per sample. We assume that the analog signal $f(t)$ is bounded: $|f(t)| \le A$. The quantization step-size is $\Delta = A/(2^{n-1})$.

innovation (ROI), or the number of parameters specifying the signal per unit time interval, is finite, these classes of signals are known as *FRI signals*. These signals can be sampled at their ROI; if the ROI is lower than the Nyquist rate, then we have sub-Nyquist sampling.

Commonly used FRI signals are streams of known pulses representing signals in time-of-flight applications, such as radar, ultrasound, optical coherence tomography, and more. An example is depicted in Figure 1 where a known transmit pulse $h(t)$ reflects from sparsely located L point targets. The received signal is given by

$$f(t) = \sum_{\ell=1}^{L} a_\ell h(t - t_\ell) \tag{2}$$

where the amplitude a_ℓ and delay $t_\ell \in (0, t_{\max}]$ denote size and location of the ℓth target and $t_{\max}$ is maximum time delay. The signal $f(t)$ is specified by $2L$ parameters, $\{a_\ell, t_\ell\}_{\ell=1}^{L}$, and hence is an FRI signal. The Nyquist rate of these signals depends on the essential bandwidth of the pulse $h(t)$, which is generally very high due to its short time duration. However, due to the FRI nature, the parameters can be determined from sub-Nyquist samples.

In Figure 2, we depict a frequently employed FRI sampling and reconstruction framework consisting of a sampling block and a reconstruction block. The sampling kernel $g(t)$ acts like an antialiasing filter in band-limited sampling and plays a key role in the sampling block. The kernel removes additional information from the FRI signal and ensures that the filtered output $y(t) = (f * g)(t)$ is in a form such that the FRI parameters can be uniquely determined from low-rate samples of $y(nT_s)$. The reconstruction block typically consists of a DSP unit that linearly combines samples of $y(nT_s)$ and a parameter estimation method that determines the FRI parameters $\{a_\ell, t_\ell\}_{\ell=1}^{L}$.

The sampling and reconstruction blocks are interdependent and must be designed in unison. To elaborate on this, we consider a compactly supported sum-of-sincs (SOS) kernel, with the impulse response given as [26]

$$g(t) = \text{rect}\left(\frac{t}{T_g}\right) \sum_{k=-K}^{K} e^{jk\omega_0 t} \tag{3}$$

where $\omega_0 > 0$ and $(t/T_g) = 1$ for $t \in [0, T_g]$ and zero elsewhere. If the support of the filter T_g is sufficiently larger than that of the signal $f(t)$, then a part of the filtered signal can be written as

$$y(t) = \sum_{k=-K}^{K} F(k\omega_0)\, e^{-jk\omega_0 t} \tag{4}$$

where $F(\omega)$ is the continuous-time Fourier transform (CTFT) of $f(t)$ (see [26] and [27] for details). By choosing $K \geq L$ and measuring $2K+1$ or more uniform samples $y(nT_s)$, one can determine the Fourier samples $F(k\omega_0)$ uniquely, provided that $\omega_s = (2\pi/T_s) \geq (2K+1)\omega_0$.

From the Fourier samples, one can construct the following sequence:

$$S(k\omega_0) = \frac{F(k\omega_0)}{H(k\omega_0)} = \sum_{\ell=1}^{L} a_\ell e^{jk\omega_0 t_\ell}, \quad k = -K, \ldots, K \tag{5}$$

where $F(\omega)$ and $H(\omega)$ are CTFTs of $f(t)$ and $h(t)$, respectively, and ω_0 is the sampling interval in the Fourier domain. The sequence $S(k\omega_0)$ consists of a linear combination of complex exponentials with discrete frequencies $\{\omega_0 t_\ell\}_{\ell=1}^{L}$. The parameters $\{a_\ell, t_\ell\}_{\ell=1}^{L}$ can be uniquely determined from the sequence $S(k\omega_0)$ by using high-resolution spectral estimation methods [31, Ch. 4], provided that $\omega_0 t_{\max} < 2\pi$ and $K \geq L$. In this approach, we assume that $H(k\omega_0) \neq 0$, $k = -K, \ldots, K$, which can always be ensured in practice, as $h(t)$ has a narrow duration in time and, therefore, large bandwidth.

Similar spectral estimation-based reconstruction can also be achieved by using a low-pass filter or a Gaussian kernel [24]. However, these kernels have infinite support and, hence, are impractical to realize. Other choices of compactly supported sampling kernels include polynomial and exponential-generating kernels [25]. All the kernels have a common working principle: spread the information of the FRI pulses such that each sample of the filtered signal contains sufficient information about the amplitude and time delays of all the pulses.

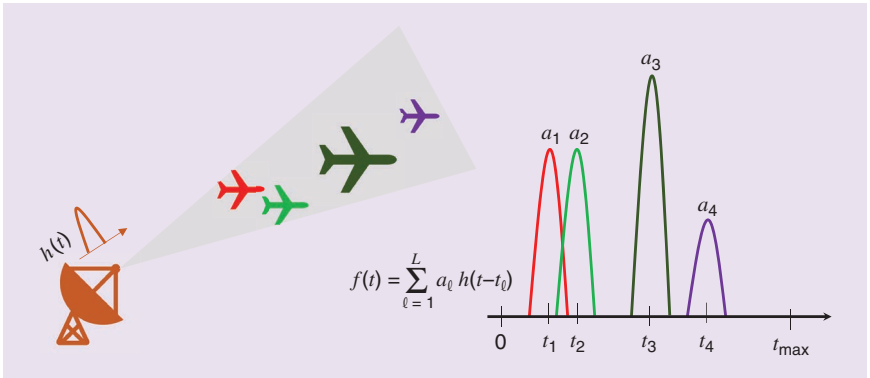


FIGURE 1. The application of FRI signals in radar imaging. A known transmit pulse $h(t)$ is reflected from sparsely located targets; the received signal is modeled as in (2) where time delays and amplitudes parameterize the signal.

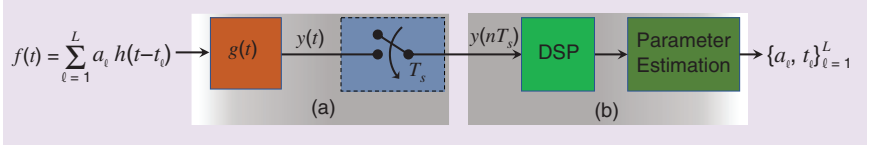


FIGURE 2. (a) FRI sampling and (b) the reconstruction framework.

From the inequalities $\omega_s = 2\pi/T_s \geq (2K+1)\omega_0$ and $|\omega_0 t_{\max}| < 2\pi$, we infer that the lowest possible sampling rate is $(2L+1)(2\pi/t_{\max})$. The sampling rate is independent of the bandwidth of the FRI signal and a function only of the number of pulses and maximum time delay. Indeed, this results in sub-Nyquist sampling, as illustrated in the subsequent example. In Figure 3, we show a particular example of an FRI signal, where $h(t)$ is a time-limited pulse constructed from a time-scaled third-order B-spline function. The FRI signal consists of $L = 5$ pulses with a maximum time delay of 1 s. The magnitude spectra of the pulse $h(t)$ and $f(t)$ show that the essential bandwidth is 200 Hz, which shows that the Nyquist rate is 400 Hz. However, by using the FRI nature of the signal, we know that it can be sampled at a minimum rate of $2L+1$, or 11 Hz. Hence, there is a reduction in the sampling rate by 36 times in this example, and consequently, the power saving will be of the same order. However, one may not achieve such a large sampling rate reduction in practice, due to noise and other practical limitations, such as nonideal sampling kernels. For example, hardware prototypes for sub-Nyquist radar systems, where the sampling and reconstruction are based on the FRI principle, are discussed in [13]. A hardware board is shown in Figure 4(a). The hardware prototypes demonstrate that using the received signals' FRI nature, the radar targets are estimated from the samples measured at 1/30 of the Nyquist rate. As the sampling rate is reduced by a factor of 30 in this case, following (S3), the power consumption is reduced by at least a factor of 30. If the operating frequencies are in the range of a few hundred megahertz, then the power consumption goes down further, as discussed earlier, with the help of FOM_W.

Sub-Nyquist sampling of multiband signals

To simultaneously communicate several band-limited signals over a common channel, signals are modulated to different carrier frequencies, as demonstrated in Figure 5. Following the Shannon–Nyquist sampling framework, such multiband signals can be sampled at twice the maximum frequency bandwidth of the signal. However, as in the example in Figure 5, the signal's spectrum is zero over several intervals, and the information bearing part resides in a few bands. Mathematically, consider a set of N disjoint frequency intervals $\mathcal{M} = \cup_{n=1}^{N} [\omega_{b_n} - \omega_{a_n}] \subset [0, 2\pi/T_{\text{Nyq}}]$, where ω_{a_n} and ω_{b_n} denote lower and upper band edges of the nth band. Then, $\mathcal{B}_{\mathcal{M}}$ denotes a set of signals whose spectrum is restricted to the interval $\mathcal{M}$. Specifically, if $f(t) \in \mathcal{B}_{\mathcal{M}}$, then $F(\omega) = 0$, $\omega \notin \mathcal{M}$. The Nyquist rate of the signals in this class is $1/T_{\text{Nyq}}$, which could be much larger than the spectral support $|\mathcal{M}|$.

By observing the sparsity of the signal's spectrum, Landau [32] showed that a multiband signal is uniquely identifiable from its stable samples measured at a rate equal to its spectral support (referred to as the *Landau rate*). Hence, for signals in $\mathcal{B}_{\mathcal{M}}$, sampling at a rate $|\mathcal{M}|$ is sufficient. Periodic nonuniform sampling and multicoset sampling patterns can be used for sampling and reconstructing multiband signals [28], [29]. Most of these approaches show that perfect reconstruction can be

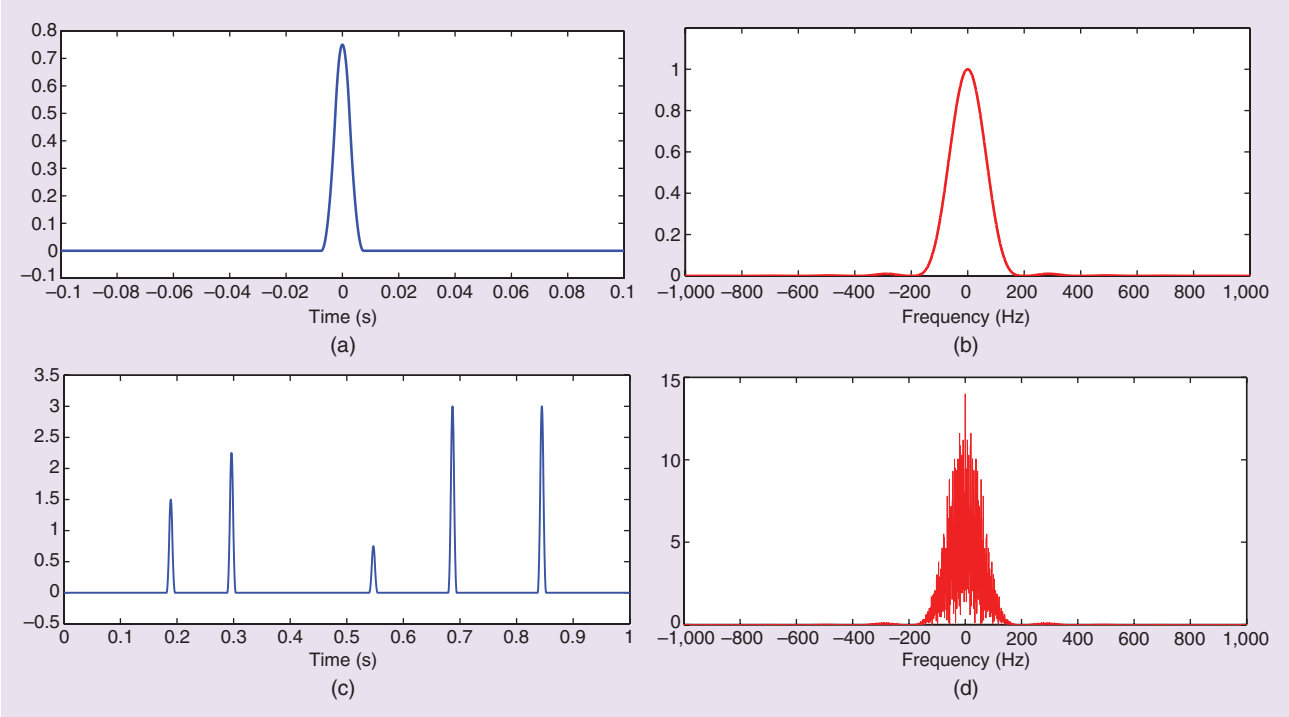


FIGURE 3. The sub-Nyquist sampling of FRI signals. (a) A time-limited pulse $h(t)$ and (b) its magnitude spectrum $|H(\omega)|$. (c) An FRI signal consisting of $L = 5$ delayed copies of $h(t)$, with $t_{\max} = 1$ s. (d) The magnitude spectrum of $f(t)$ shows that the Nyquist sampling rate is 400 Hz; however, the FRI-based framework requires sampling at 11 Hz.

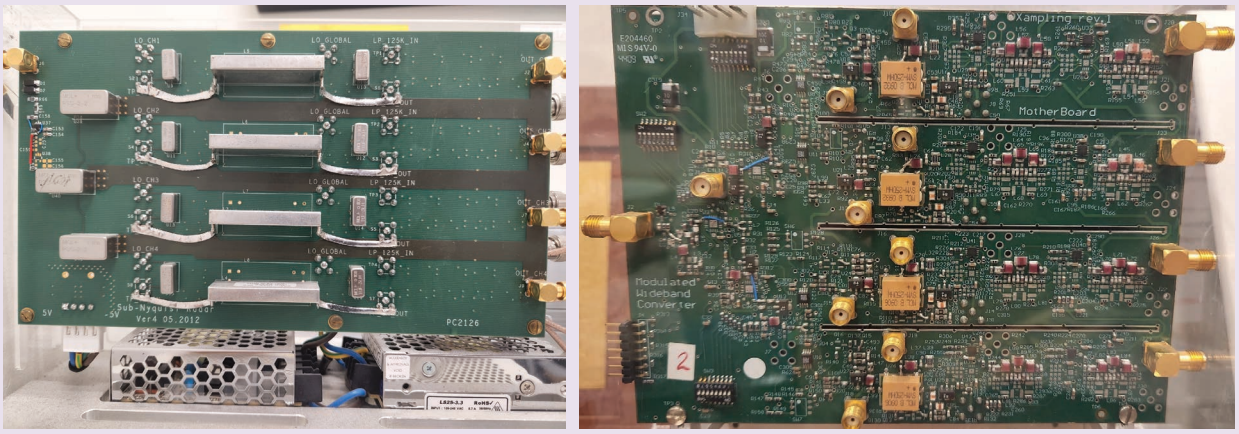


FIGURE 4. (a) A hardware prototype of a sub-Nyquist radar [13]. (b) A hardware realization of the MWC consisting of $M = 4$ channels [14], [15].

achieved by sampling the signals at the Landau rate, provided that the band edges $\{\omega_{a_n}, \omega_{b_n}\}_{n=1}^{N}$ are known.

A blind sampling and reconstruction framework was presented in a series of papers [14], [30], where the authors proved that the minimum sampling rate is twice Landau's rate and not more than the Nyquist rate in the blind setup. In these blind multiband works, the authors assumed that $\omega_{b_n} - \omega_{a_n} = 2\pi B$ and B and N are known. Then, the set of multiband signals can be uniquely identifiable from stable samples measured at a rate $\min\{2NB, 1/T_{\text{Nyq}}\}$. An oversampling by a factor of two is the price paid for blindness. The signal reconstruction algorithms in these works first estimate the unknown spectral supports and then use a conventional algorithm to reconstruct the signals from the samples. For support recovery, the algorithms rely on a similar principle as in FRI sampling: to spread or mix the information so that the desired information is determined from fewer samples relying on notions from compressed sensing.

For mixing the information, the authors proposed two multichannel frameworks that are based on multicoset sampling [29]: the quadrature analog-to-information converter (QAIC) [33], [34] and modulated wideband converter (MWC) [14], [15]. The principal idea of mixing is based on aliasing of the spectrum. Reconstruction is achieved by applying sparse recovery methods from compressive sensing [35], as discussed next. For an M-channel sampling framework, an MWC-based mixing and sampling framework is presented in Figure 6. The mixing is performed by multiplying $f(t)$ with a set of M periodic signals $p_m(t) = \sum_{l=-\infty}^{\infty} c_{m,l} e^{j\omega_s t}, m = 1, \ldots, M$, where $\omega_s \geq 2\pi B$ and $c_{m,l}$ are Fourier coefficients of the periodic signals. This results in modulation in the frequency domain, and as a result, the low-pass spectrum of the product $f(t)p_m(t)$ is a linear combination of all the bands, as evident in Figure 6(c). The mixed spectrum is captured from the sampled signal by passing the product $f(t)p_m(t)$ through a low-pass filter and then sampling uniformly at its Nyquist rate. The discrete-time Fourier transform (DTFT) of the samples is related to the spectrum of the continuous-time multiband signal, as [30]

$$F_m(e^{j\omega T_s}) = \sum_{\ell=-L}^{L} c_{m,\ell} F(\omega - \ell\omega_s), \quad \omega \in [-\omega_s/2, \omega_s/2] \tag{6}$$

where $\omega_s = 2\pi/T_s < \omega_{\text{Nyq}}$ is the sampling rate in radians per second. The summation in (6) is due to aliasing because of sub-Nyquist sampling, and its finiteness is a consequence of the band limitedness of $f(t)$. Rewriting (6) in matrix–vector notation, we have

$$\mathbf{y}(\omega) = \mathbf{A}\mathbf{x}(\omega) \in \mathbb{C}^M, \quad \omega \in [-\omega_s/2, \omega_s/2] \tag{7}$$

where $\mathbf{A}_{m,\ell} = c_{m,\ell}$, $\mathbf{y}(\omega) = [F_1(e^{j\omega T_s}), \ldots, F_M(e^{j\omega T_s})]^{\mathrm{T}}$ and $\mathbf{x}(\omega) = [F(\omega - L\omega_s), \ldots, F(\omega + L\omega_s)]^{\mathrm{T}} \in \mathbb{C}^{2L+1}$. The sparsity of the spectrum $F(\omega)$ ensures that the vector $\mathbf{x}(\omega)$ is sparse for each $\omega \in [-\omega_s/2, \omega_s/2]$, provided that $\omega_s \geq 2\pi B$ [see Figure 6(d)]. Algorithms and conditions for recovering $\mathbf{x}(\omega)$

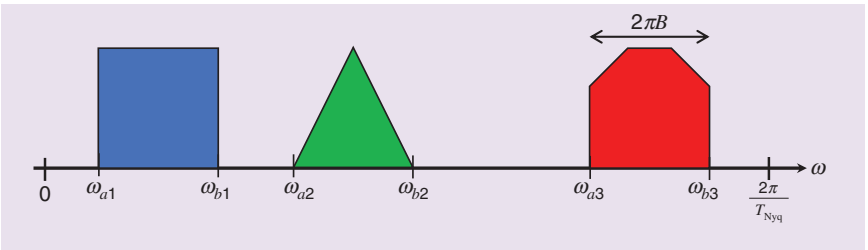


FIGURE 5. The spectrum of a multiband signal consisting of three disjoint bands. The maximum frequency of the signal is $2\pi/T_{\text{Nyq}}$, and the Nyquist rate is $1/T_{\text{Nyq}}$ Hz. In this example, for simplicity, we consider a signal with a positive spectrum, whereas signals in practice can have both positive and negative parts.

from $\mathbf{y}(\omega)$ are derived in [30], where the authors show that the minimum number of hardware channels should be greater than the number of bands; that is, $M \geq 2N$. Hence, for reconstruction, the minimum sampling rate is $2NB$, which is twice the rate for unique identifiability. In practice, the number of channels can be reduced below $2N$, and as low as one channel, by designing a specific set of periodic signals $p_m(t)$ [30].

The periodic signals in an MWC are typically realized using a sign-alternating sequence, or pseudorandom noise (PN) sequence, generator. The PN sequence has to alternate signs a sufficiently large number of times within a time period to ensure that the sparse spectrum is estimated from the compressed measurements. Thus, these PN mixers operate at the Nyquist rate of the maximum input signal frequency. For example, for the multiband signal in Figure 5, the mixers operate at $2\pi/T_{\text{Nyq}}$. By codesigning the analog preprocessing with DSP, the QAIC applies a bandpass filter and downconverts the high-frequency input signal. Specifically, by assuming that the spectra of the multiband signal lie in a frequency interval $[\omega_{\min}, \omega_{\max}]$, where $\omega_{\max} \leq 2\pi/T_{\text{Nyq}}$ and $\omega_{\min} > 0$, the downconverted signal spectrum lies in the range $[0, \omega_{\max} - \omega_{\min}]$. With this change in the spectrum, the Nyquist rate of the signal is reduced by $\omega_{\min}$, and the same amount reduces the rate of the PN sequence. A comparison of the low-pass filter-based MWC and a bandpass filter-based QAIC is provided in Figure 7. If $\omega_{\min} \gg 0$ for the application of interest, the power savings introduced by the bandpass QAIC architecture due to the reduction of the clock rate and sequence length of the PN sequence generator compared to the low-pass MWC architecture would be significant, up to an order of magnitude for the analog preprocessing block interfacing with the sub-Nyquist sampling ADC, as demonstrated in [33].

In the FRI and multiband frameworks, the power reduction is achieved by reducing the sampling rates. However, in both these approaches, analog front ends are used to facilitate sub-Nyquist sampling. For example, in Figure 6, M channels are used, where each channel consists of a multiplier, low-pass filter, and PN sequence generator. These circuits can be built by using existing low-power circuits and, hence, do not add significant power gain to the overall circuits.

As in the case of FRI sampling, power saving is also applicable for multiband signals when the minimum sampling rate, $2NB$ Hz, is less than the Nyquist rate. Again, the savings amount depends on the actual sampling rate ratio to the Nyquist rate. In [14] and [15], Mishali et al. proposed hardware prototypes for MWC-based sub-Nyquist samplers for B = 19 MHz, N = 6, and $1/T_{\text{Nyq}} = 2$ GHz; the signals can be sampled and reconstructed at a rate of 280 MHz by using an M = 4-channel MWC [see Figure 4(b)]. By using the multiband structure, there is a sevenfold reduction in the sampling rate, which reduces the power requirements of the ADC by the same amount.

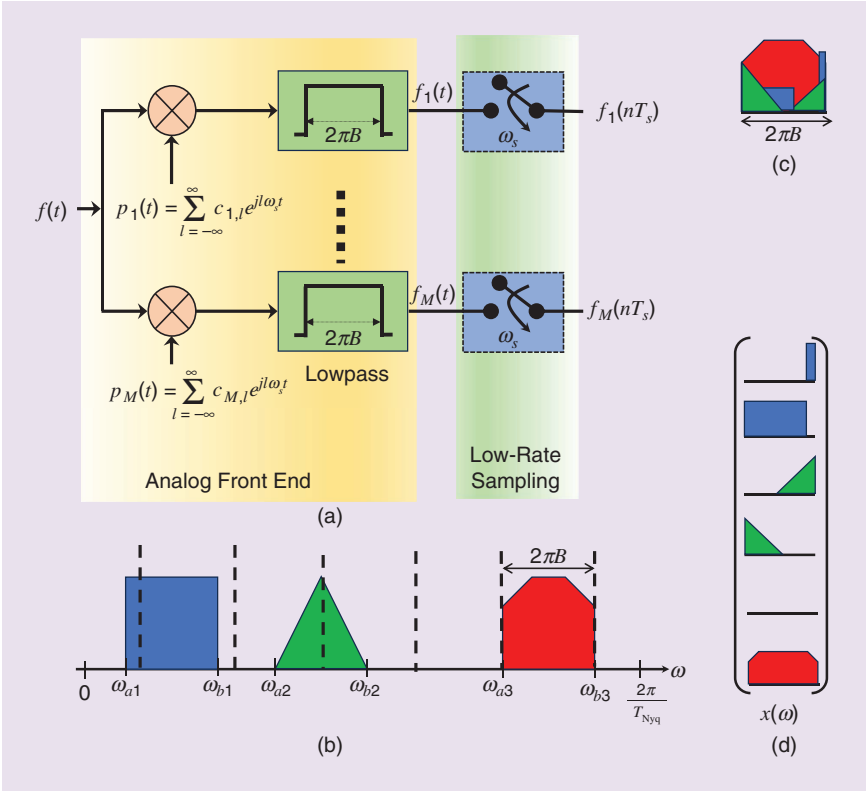


FIGURE 6. An M-channel MWC-based mixing and sub-Nyquist framework for multiband signals [14], [30]. (a) The MWC architecture. (b) Multiband spectrum. (c) Spectrum of the low-pass filter output. (d) Spectrum in (c) in a vector form.

Modulo-ADC

The higher the DR of an ADC, the higher the number of bits required to keep a low quantization error, which results in high power consumption. Hence, it is desirable to keep the DR low. However, to avoid clipping due to saturation, the signal's DR must be within that of ADC's. In many applications, it is not always possible to premeditate the signal's DR and then choose an ADC with a suitable DR. Moreover, the available ADCs have a fixed DR in many scenarios. An attenuator can be applied to address these mismatches in DRs by scaling down the signal to fit into the ADC's DR. This solution may not be suitable when the amplitude of the signal varies significantly over time. For such a signal, small components of the signals are scaled down below the noise floor and, hence, cannot be detected.

Theory and algorithms

A modulo folding operation was suggested by Bhandari et al. [4] that folds the signal before sampling such that its variations are contained within the

ADC's DR. To be precise, let $f(t)$ be an analog signal to be sampled, which is bounded as $|f(t)| \le A$. The ADC's DR is $[-\lambda, \lambda]$, where $\lambda < A$. To process $f(t)$ through the ADC, it is first folded as $f_\lambda(t) = \mathcal{M}_\lambda(f(t))$, where $\mathcal{M}(\cdot)$ is the folding operation, defined as $\mathcal{M}_\lambda(a) = (a + \lambda) \bmod 2\lambda - \lambda$, for a real-valued a. The folding operation ensures that $|f_\lambda(t)| \le \lambda$. The folded signal is then sampled using a low-DR ADC, which results in measurements $f_\lambda(nT_s)$, where $1/T_s$ represents the samples per second. The folding operation does not discard any information of the analog signals; hence, the samples $f_\lambda(nT_s)$ retain necessary information of $f(t)$. In fact, mathematically, it was shown that band-limited signals are uniquely identifiable from modulo samples, provided that they are sampled above their Nyquist rate [4], [5]. Based on this discussion, the key message is that the DR of a modulo ADC—an ADC preceded by a modulo operation—is much higher (theoretically, unlimited) than the ADC's DR. Hence, the modulo-based approach is termed a *high-DR ADC*. An example of modulo folding for a band-limited signal is given in Figure 8(a), where the signal with a high DR is folded to stay within the ADC's DR.

In the preceding paragraph, we mentioned that the modulo DR's ADC is unlimited ($A/\lambda \to \infty$), provided that the sampling rate is higher than the Nyquist rate. However, in practice, recovery of $f(t)$ from the folded samples $f_\lambda(nT_s)$ depends on A/λ and T_s. Typically, the reconstruction process works in two stages: first, determine the true samples $f(nT_s)$ from the folded samples by using an unfolding algorithm, and second, use standard reconstruction to get $f(t)$ from $f(nT_s)$. For band-limited signals, the latter part requires that the sampling rate should be above the Nyquist rate. However, for unfolding, the signals are required to be oversampled, where the oversampling factor (OF = f_s/f_{Nyq}) varies from algorithm to algorithm. Here, f_{Nyq} is the Nyquist rate.

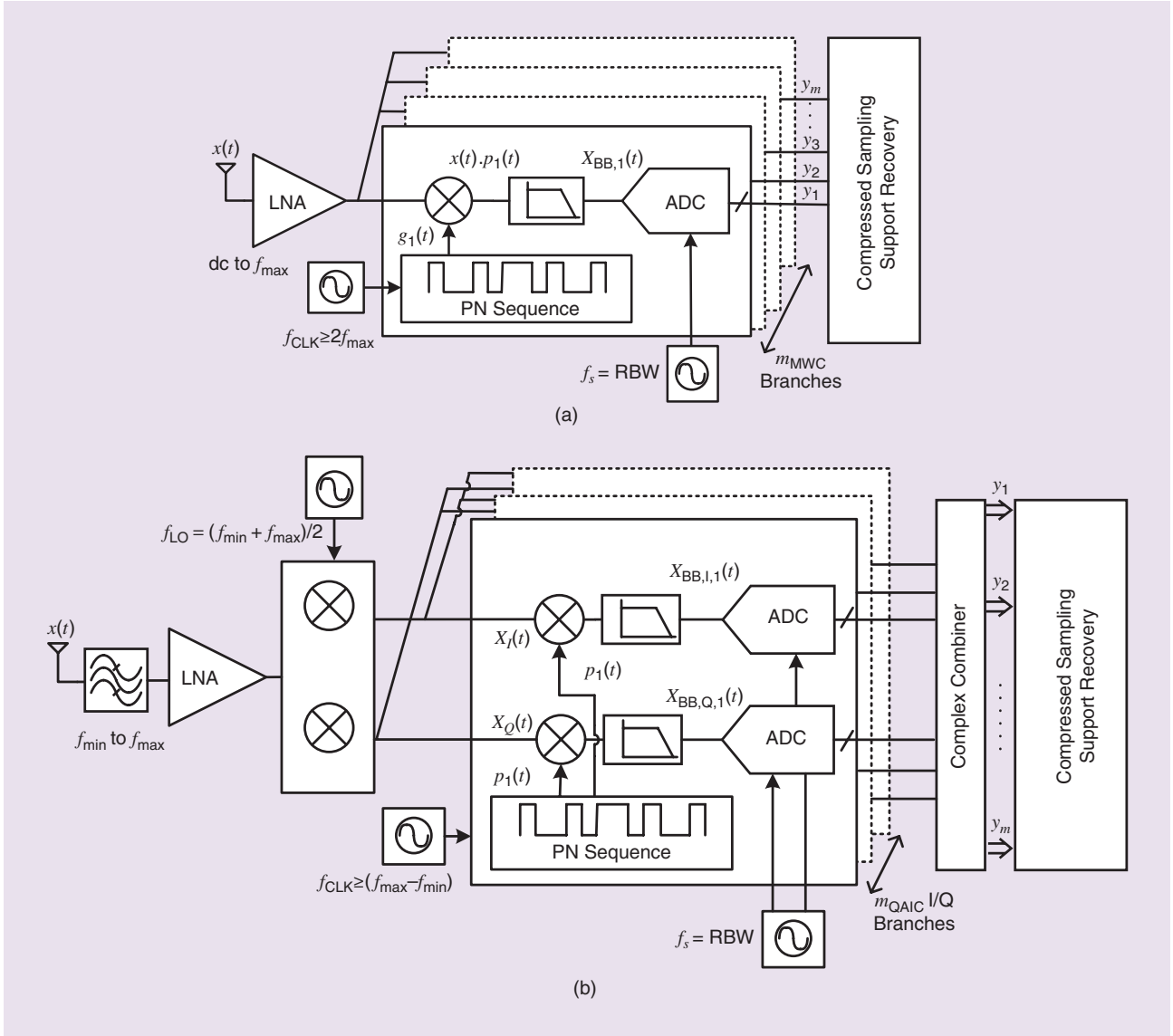


FIGURE 7. Hardware prototypes for sub-Nyquist sampling, known as *compressed sampling analog-to-information converter architectures.* (a) A low-pass MWC [14], [15]. (b) A bandpass QAIC [33], [36]. LNA: low-noise amplifier; RBW: resolution bandwidth.

Unfolding algorithms [4], [5], [6] typically use the following decomposition of the modulo signal or samples:

$$f_\lambda(nT_s) = f(nT_s) + z(nT_s) \tag{8}$$

where $z(t)$ is a piecewise constant function whose values are multiples of 2λ and hence, $z(nT_s) \in 2\lambda\mathbb{Z}$. Bhandari et al. [4] proposed a higher-order differences approach for unfolding. Let $\triangle^d$ be the dth-order sample difference operator. Then, we have that $\mathcal{M}_\lambda(\triangle^d f_\lambda(nT_s)) = \mathcal{M}_\lambda(\mathcal{M}_\lambda(\triangle^d f(nT_s)) + \mathcal{M}_\lambda(\triangle^d z(nT_s)))$. The second term is zero, as $\triangle^d z(nT_s) \in 2\lambda\mathbb{Z}$. Hence, if

$$\left|\triangle^d f_\lambda(nT_s)\right| < \lambda \tag{9}$$

then we get $\mathcal{M}_\lambda(\triangle^d f_\lambda(nT_s)) = \triangle^d f(nT_s)$. In other words, we can determine the dth-order difference of the true samples from the folded samples, provided that (9) is satisfied. The authors of [4] showed that the condition is satisfied for OF ≥ 17, and they proposed an approach to recover $f(nT_s)$ from higher-order differences. The sampling rate is high for this algorithm, and the use of sample differences makes it unstable in the presence of noise.

A robust and sample-efficient algorithm is proposed in [5], where the authors used band limitedness and decay properties of the samples $f(nT_s)$ to extract them from $f_\lambda(nT_s)$. The main idea of the method and the corresponding optimization problem are discussed in "Beyond-Bandwidth Residue Recovery Algorithm." In this algorithm, for an acceptable accuracy of the reconstruction, the OF varies between two and eight, depending on the ratio $\theta = A/\lambda$ and the noise level. The modulo ADC framework can also be extended to FRI and other classes of signals [6], [16]. For example, for the FRI sampling framework, a modulo folding operation is applied after the filtering stage (see Figure 2), and an unfolding algorithm is used before the DSP block. As in the band-limited case, it is required to sample above the ROI for FRI signals when using a modulo ADC. As a consequence, FRI sampling with a modulo ADC falls under the sub-Nyquist framework.

Power analysis of modulo ADC

We derive theoretical lower bounds on the power consumption of a modulo ADC and compare it with a conventional ADC. To this end, we consider a conventional ADC with sampling rate f_s (which is equal to the Nyquist rate for a band-limited signal or equal to the ROI for an FRI signal) and input signals DR A, as in Figure 9. For a n-bit flash-type quantizer, the total power consumption is given by (S3), which is also indicated in the table in Figure 9. To determine the power of the modulo ADC, we determine the power consumption of its constituents: a modulo folding circuit and a conventional low-DR ADC (see Figure 9). The low-DR ADC has a DR range $[-\lambda, \lambda]$ with n-bit resolution and operates at an oversampling rate OF f_s. Following the derivations presented in the "Power Consumption of an ADC and FOMs" section and assuming that the capacitance values of the low-DR ADC are the same as those of the conventional ADC, the power of the sampler and the comparator of the low-DR ADC are given as

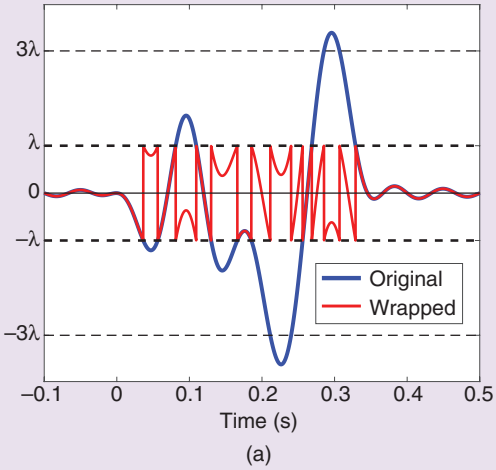
$$\frac{24kT\text{OF}f_s 2^{2n}}{\theta^2} \text{ and } \frac{4n\ln 2\text{OF}f_s C_C 2\lambda V_{\text{eff}}}{\theta}$$

respectively. By comparing these expressions with those of the conventional ADC, we note that the power consumption of the low-DR ADC P is given as

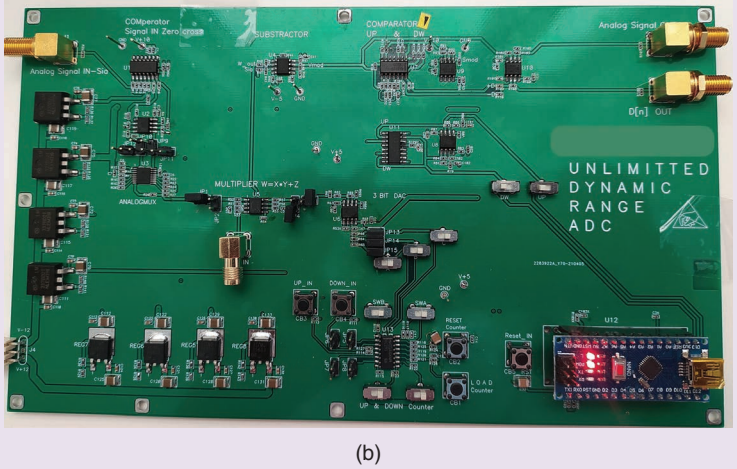
$$P = \frac{\text{OF}}{\theta^2} P \tag{10}$$

where $P = P_S + P_C$ is the power of a conventional ADC.

From the analysis up to this point, we infer that for OF $< \theta^2$, the sample and hold (S/H) with the quantization part of a modulo ADC consumes less power than a conventional ADC. For



(a)



(b)

FIGURE 8. (a) The modulo folding of a band-limited signal. The ADC's DR is $[-\lambda, \lambda]$, and the signal is folded to stay within the range. (b) A hardware prototype of a modulo ADC.

Beyond-Bandwidth Residue Recovery Algorithm

We give a brief overview of the beyond-bandwidth residue recovery algorithm [5] that can be used to unfold band-limited signal samples. In the discussion, we assume that signals have finite energy and are band limited to frequency interval $[-\omega_{\text{Nyq}}, \omega_{\text{Nyq}}]$. In addition, we assume that the sampling rate is above the Nyquist rate; that is, $\omega_s > 2\omega_{\text{Nyq}}$. The following two properties of a finite-energy band-limited signal are used in this algorithm:

1) *Time-domain decay property*: From the Riemann–Lebesgue lemma, we have that $\lim_{|t|\to\infty} f(t) = 0$. The time-domain decay implies that for every $\lambda > 0$, there exists an integer N_λ such that $|f(nT_s)| < \lambda$ for all $|n| > N_\lambda$.
2) *Frequency-domain decay property*: Since the signal is sampled above the Nyquist rate, the DTFT of the samples $f(nT_s)$ is zero beyond the bandwidth; mathematically, $F(e^{j\omega T_s}) = 0$ for $\omega_{\text{Nyq}} < |\omega| < \omega_s/2$.

By using the decomposition in (8) and the time-domain decay property, we have that $z(nT_s) = 0, |n| > N_\lambda$, as $f_\lambda(nT_s) = f(nT_s)$ for those samples.

Further, by using the band limitedness of the samples, we get $F_\lambda(e^{j\omega T_s}) = Z(e^{j\omega T_s})$, $\omega \in \rho = (-\omega_s/2, -\omega_{\text{Nyq}}) \cup (\omega_{\text{Nyq}}, \omega_s/2)$. Hence, the samples of the residue are compactly supported over $n \in [-N_\lambda, N_\lambda]$, and the DTFT is known over a finite-length interval ρ. Let vectors $\mathbf{f}_\lambda, \mathbf{z} \in \mathbb{R}^{2N_\lambda+1}$ denote samples $f_\lambda(nT_s)$ and $z(nT_s)$, respectively, for $n \le |N_\lambda|$. In addition, let $\mathcal{F}_\rho$ be a partial DTFT operator that evaluates Fourier measurements at frequencies in the set ρ. Then, from the above discussion, we can write the following optimization problem

$$\min_{\mathbf{z}} \; C(\mathbf{z}) = \frac{1}{2}\left\| \mathcal{F}_\rho \mathbf{f}_\lambda - \mathcal{F}_\rho \mathbf{z} \right\|^2 \quad \text{subject to} \quad \mathbf{z} \in \mathcal{S}_{N_\lambda} \tag{S4}$$

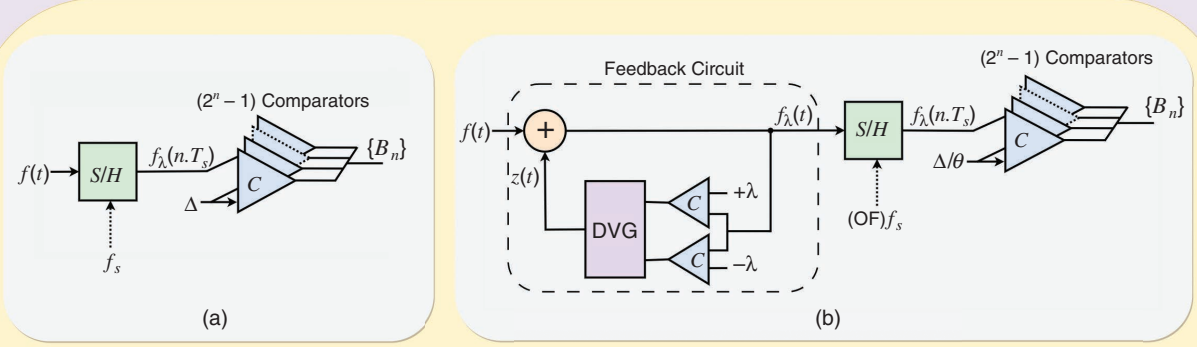
where $\mathcal{S}_{N_\lambda}$ is a set of sequences that have support on the interval $[-N_\lambda, N_\lambda]$.

Problem (S4) can be solved using a projected gradient descent method, starting from an initial point $\mathbf{z}^0 \in \mathcal{S}_{N_\lambda}$. The steps at the kth iteration are

$$\begin{aligned} \mathbf{y}^k &= \mathbf{z}^{k-1} - \gamma_k \nabla C(\mathbf{z}^{k-1}) \\ \mathbf{z}^k &= P_{\mathcal{S}_{N_\lambda}}(\mathbf{y}^k) \end{aligned} \tag{S5}$$

where $\gamma_k > 0$ is a suitable step-size, $\nabla C(\mathbf{z}) = \mathcal{F}_\rho^* \mathcal{F}_\rho(\mathbf{z} - \mathbf{f}_\lambda)$ is the gradient of $C(\mathbf{z})$, and $P_{\mathcal{S}_{N_\lambda}}(\cdot)$ is the orthogonal projection onto $\mathcal{S}_{N_\lambda}$.

After estimating $z(nT_s)$ from the modulo samples, the unfolded samples are determined by (8).



	Conventional ADCs	Modulo Sampling ADC
Quantization Noise	$\frac{4A^2}{12} 2^{-2n}$	$\frac{4\lambda^2}{12} 2^{-2n}$
Resolution (Bits)	n	n
Sampling Power	$P_S = 24\ kT f_s 2^{2n}$	$\left[24\ kT\ (\text{OF}) f_s 2^{2n}\right]/\theta^2$
Comparator Power	$P_C = 2n \ln 2\, f_s\, C_C (2A)\, V_{\text{eff}}$	$\left[2n \ln 2\ (\text{OF}) f_s\, C_C (2\lambda)\, V_{\text{eff}}\right]/\theta$
Total Power	$P_S + (2^n - 1)\, P_C$	$\text{OF}\, \frac{P_S + (2^n - 1)\, P_C}{\theta^2} + P_{\text{FB}}$

(c)

FIGURE 9. The power consumption in (a) a conventional flash ADC and (b) a modulo sampling flash ADC. (c) Power comparision of the conventional ADC and the modulo-sampling ADC. DVG: digital voltage generator; S/H: sample and hold.

example, in the modulo ADC hardware prototype presented in [17], $\theta \leq 8$ and OF ≤ 5, which is a power consumption reduction by a factor of 12.8. However, the feedback circuitry of a modulo ADC will add additional power requirements, which we consider next.

The goal of the modulo circuit, or the feedback circuit, is to fold an input signal $f(t) \in [-A, A]$ to a DR $[-\lambda, \lambda]$. The circuit consists of two comparators and a digital voltage generator (DVG). The input to the comparators is the modulo signal $f_\lambda(t)$. The comparators trigger whenever their input signal crosses $\pm\lambda$. The DVG reacts to the trigger signals and generates a residual signal $z(t) \in 2\lambda\mathbb{Z}$, which is added to the input signal to keep it within $[-\lambda, \lambda]$. Hence, we focus on the power utilization of the capacitors and the DVG. To this end, it is required to find an expression of the operating frequency f_{FB} of the feedback loop. The frequency f_{FB} depends on how fast the capacitors have to switch, and it could be higher than the sampling rate of the ADC ($= \text{OF} f_s$). Specifically, for any signal $f(t)$, f_{FB} denotes an upper bound on the number of times it crosses amplitude levels $\pm(2m+1), m \in N$. To derive an upper bound in f_{FB} for a band-limited signal, we use the fact that the number of zeros of a band-limited function is equal to the Nyquist rate. Then, by using a derivation similar to that in [6, Appendix], it can be shown that $f_{\text{FB}} = 2\theta f_{\text{Nyq}}$, where f_{Nyq} is the Nyquist rate. Based on f_{FB}, the power consumption of the comparators can be modeled similarly to (S2). However, the power consumption of the comparator is proportional to $\ln\theta$ instead of $2n\ln 2$ since the comparators need to resolve the voltage of 2λ and generate a voltage level of A at the output. Therefore, we rewrite the lower bound as (11), where $C_{C,\text{FB}}$ is the latch comparator load capacitance. The power consumption of the DVG is modeled as the power consumption of a capacitive digital-to-analog converter (C-DAC) since it scales down or up the output voltage in multiples of 2λ with reference voltage A. We estimate the average power consumption of the DVG as (12), where C_{DAC} and N are the total C-DAC capacitance and bit resolution of the C-DAC in the feedback circuit, respectively [37]:

$$P_{C,\text{FB}} = \ln\theta f_{\text{FB}} C_{C,\text{FB}} V_{\text{eff}} A \tag{11}$$

$$P_{\text{DVG}} = P_{\text{DAC}} = 0.66 \frac{f_{\text{FB}} C_{\text{DAC}} A^2}{N+1} \tag{12}$$

$$P_{\text{FB}} = P_{\text{DVG}} + 2P_{C,\text{FB}}. \tag{13}$$

The total power consumption of the feedback circuit in (13) is the sum of the DVG and two comparators. The total power consumption of the modulo ADC is given as

$$P_{\text{modulo ADC}} = P' + P_{\text{FB}} = \frac{\text{OF}}{\theta^2} P + P_{\text{FB}}. \tag{14}$$

For a fixed f_s, A, and n, we note that power reduction in the sampling and quantization part of the modulo ADC is inversely proportional to θ^2, whereas that in the modulo circuit is proportional to $\theta\ln\theta$. The capacitance of the C-DAC can be minimized to reduce the power consumption of the DVG of a modulo circuit under the noise and linearity limitations. For example, with a unit capacitance value of 10 fF, a 4-bit C-DAC can be used that allows up to $\theta = 16$. In this case, we have $C_{\text{DAC}} = 2^4(10\text{ fF}) = 160$ fF. Now, if A and f_{FB} are assumed to be in the 3.3-V and 10-MHz ranges, respectively, this results in $P_{\text{DVG}} \simeq 2.3\ \mu$W, which is much less compared to the power consumption of the state-of-the-art ADC in [21] that operates close to this frequency range. Hence, by carefully optimizing the feedback circuit, a modulo ADC can have lower power requirements compared to a conventional ADC for any $\theta > 1$.

In the context of power saving for a modulo ADC, we would also like to emphasize that the OF, which depends on the unfolding algorithm, may not be independent of θ. In fact, as shown via simulations in [5], the OF for most algorithms increases with θ. In such cases, the power saving in a modulo ADC still holds if the OF does not increase faster than θ^2. Hence, designing sample-efficient algorithms plays a key role in the power saving aspect of a modulo ADC.

A few works presented hardware prototypes of modulo ADCs [16], [17]. The emphasis in these works is to show that one can fold the analog signal to a low DR and the applicability of the unfolding algorithms. In [16], the authors considered different signal models, hardware limitations, and algorithms; however, they did not provide details of the hardware implementation. Moreover, the results are presented for signals up to 300 Hz. A hardware prototype for signals up to 10 kHz, with detailed circuitry, is presented in [17, Fig. 4]. The authors showed that for FRI signals, the system operates six times below the Nyquist rate, and the modulo ADC can sample signals that are eight times larger than the ADC's DR.

The modulo ADC described in this work reduces the DR of the input signal, allowing for fewer bits to be used for a given quantization step-size and error margin. However, this reduction comes at the cost of the oversampling required for signal unfolding. This strategy of employing a higher sampling rate with fewer bits is analogous to predictive coding techniques, such as delta modulation, differential pulse-code modulation, and sigma–delta modulation.

In particular, sigma–delta ADCs prioritize high resolution by employing oversampling and noise shaping techniques, rather than optimizing for power efficiency through coarse quantization. In sigma–delta ADCs, the input signal is sampled at a rate significantly higher than the Nyquist rate, spreading quantization noise over a broader frequency range. Noise shaping feedback loops shift this noise toward higher frequencies, outside the signal band of interest, where it is attenuated using digital decimation filters. While this approach achieves high resolution, it comes at the cost of increased complexity and power consumption due to the need for high-speed clocks, digital filters, and the computational overhead associated with oversampling. A detailed analysis of sigma–delta ADC operation and efficiency, however, falls beyond the scope of this article.

It is essential to recognize that ADC power consumption is proportional to the product $f_s 2^n$, where f_s is the sampling

rate and n is the number of quantization bits. In sigma–delta and modulo ADCs, increasing the sampling rate raises the power consumption linearly, while reducing the number of bits decreases it exponentially. As a result, predictive coding methods, including sigma–delta and modulo ADC approaches, can offer power savings compared to conventional ADCs operating at the Nyquist rate with higher bit depths. However, the added complexity of the circuitry, particularly in modulo folding and sigma–delta decimation, can offset some of the power savings.

Although a precise calculation of the additional power required for predictive coding schemes is beyond the scope of this discussion, a high-level comparison between modulo ADC and sigma–delta converters can be found in [38]. The authors emphasize the simplicity of the modulo ADC encoder and the discrete nature of its decoding process, contrasting it with the feedback-based complexity of sigma–delta converters. A more detailed comparison of the power efficiency, complexity, and other factors involved in modulo ADCs and other predictive coders remains an open area of research.

Event-based sampling

The sampling approaches discussed in the previous sections are based on uniform sampling, where a continuous-time signal $f(t)$ is represented by $f(nT_s), T_s > 0, n \in \mathbb{Z}$. A key advantage of uniform sampling is that it allows the application of standard Fourier analysis. This, in turn, relates the spectra of $f(t)$ and $f(nT_s)$ and often leads to closed-form expressions for reconstruction, such as Shannon–Nyquist recovery. Despite being widely used, a shortcoming of uniform sampling is that it measures samples at the same rate, usually dictated by the maximum signal component, and ignores whether the signal is changing rapidly or not locally. Specifically, the instantaneous bandwidth of most real-world signals varies across time, even if the signals' overall bandwidth is fixed. In such scenarios, it is power efficient to measure samples at a low rate in regions with small changes and vice versa.

To this end, event-based samplers, such as level-crossing sampling [7] and integrated and fire time-encoding machines (IF-TEMs) [9], [10], [39], are applied where the sampling locations are a function of the analog signal. In these frameworks, analog signals are represented by a set of time instants $\{t_n\}$ instead of their values at specific time instants as in uniform and random sampling. For example, in a popular level-crossing sampling architecture called the *zero-crossing detector*, the signal is represented by its zero-crossing instants [7]. In general level crossing, a signal is represented by time instants at which the signal crosses a set of predefined amplitude levels. Moreover, level crossing-based approaches offer the additional advantage of providing information about the signal's behavior between two consecutive sampling instants, specifically that it remains within a defined range. This "no event" information, which is unavailable in conventional Shannon–Nyquist sampling, can significantly enhance the accuracy of signal reconstruction [40].

Theory and algorithms

The level crossing-based approach can be implemented using multiple comparators, with one assigned to each level. However, this method introduces substantial hardware complexity, reducing its efficiency for practical applications. More power-efficient implementations, utilizing only two comparators, have been demonstrated [41], [42]. Additionally, architectures based on digital comparators have also been proposed [43]. Despite these advancements, this article focuses primarily on conventional analog comparator-based implementations.

In comparison to level crossing-based ADCs, IF-TEMs use a single comparator to time encode analog signals. In an IF-TEM, an analog signal $f(t)$ is added to a bias b such that $b + f(t) \geq 0$. This is ensured by choosing the bias as $b > A$, where $|f(t)| \leq A$. Thus, bias b is determined by the input signal DR. The positive signal is scaled as $(1/\kappa)(b + f(t))$, where $\kappa > 0$, and then integrated. The resulting signal is compared with a threshold Δ, as illustrated in Figure 10(a). When the value of the output of the integrator reaches threshold Δ, defined by the input signal level, bias b, and signal bandwidth, the time instant is recorded, and the integral is reset. The process is repeated to get the time encodings $\{t_n\}$, which are digital representations of $f(t)$ and are a function of IF-TEM parameters $\{b, \kappa, \Delta\}$. As discussed next, the reconstruction of $f(t)$ is based on nonuniform sampling-based recovery methods.

Following the sampling mechanism of the IF-TEM discussed above, $f(t)$ and its time encodings are related as

$$\frac{1}{\kappa}\int_{t=t_{n-1}}^{t_n} (b + f(t))\,\mathrm{d}t = \Delta. \tag{15}$$

From this equation and by using the boundedness $|f(t)| < c$, the difference between consecutive firings is related as

$$\frac{\kappa\Delta}{(b+A)} \leq t_n - t_{n-1} \leq \frac{\kappa\Delta}{(b-A)}. \tag{16}$$

By using these bounds, the maximum and minimum number of time encodings per second, or the *firing rate* (*FR*), are given as

$$\mathrm{FR}_{\max} = \frac{(b+A)}{\kappa\Delta} \quad \text{and} \quad \mathrm{FR}_{\min} = \frac{(b-A)}{\kappa\Delta} \tag{17}$$

respectively. The notion of the FR has a similar meaning to that of the sampling rate in uniform sampling or the sampling density (average number of samples per second) in random sampling. The difference is that the FR is signal dependent, whereas the sampling density or rate is fixed. Specifically, the FR increases with the signal level. An illustrative example appears in Figure 10(b).

For perfect reconstruction of $f(t)$, the IF-TEM parameters should be chosen such that $\mathrm{FR}_{\min}$ is above a certain rate. For example, Lazar and Tóth [9] used an iterative algorithm for

the reconstruction of band-limited signals and showed that the algorithm converges to the true signal provided that $\mathrm{FR}_{\min}$ is above the Nyquist rate. Similarly, [10] showed that FRI signals could be reconstructed from their time encodings if the minimum FR is set above the ROI. The reconstruction approach is summarized in "Finite-Rate-of-Innovation Signal Reconstruction From Integrated and Fire Time-Encoding Machine Samples."

Power efficiency of IF-TEMs

In the following, we determine the power that an IF-TEM circuit consumes and compare it with that in a conventional ADC for the same input signal. The details of our analysis are reported in Figure 11. For the conventional ADC, we use (S3) to represent its power consumption. For the IF-TEM, we note that there are three components: 1) an adder with a bias; 2) an integrator with a reset rate αf_s, where α is a nonuniform sampling activity factor that reflects nonperiodical sampling activity; and 3) a comparator with a threshold Δ. Among these, the integrator and comparator are power-hungry blocks, and we focus on them in the following analysis.

The quantization of time encodings utilized in IF-TEMs is usually not carried out in the same way as in conventional ADCs, but specialized time-to-digital circuits (TDCs) are used [44]. The underlying principle in TDCs is that time can be divided into measurable intervals that are quantized into digital representations, or bits. There are several ways of realizing a TDC, such as analog based, counter based, or delay line (refer to [44] for details). Among these, most digital implementation-based TDCs have power consumption an order of magnitude lower than typical analog circuits. This is the reason we did not account for the TDC in the power calculation of the IF-TEM framework.

For the calculation of the power consumption, we note that the integrator can be viewed as an active S/H (a capacitor and a switch) with n = 1-bit resolution [45] since the number of

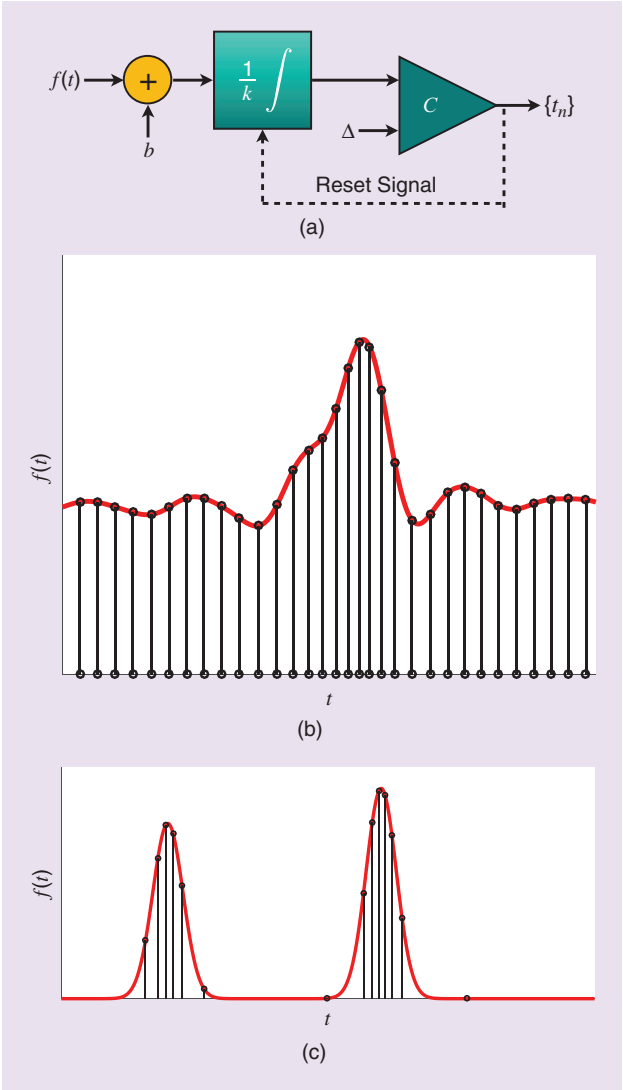


FIGURE 10. (a) An IF-TEM. (b) IF-TEM samples of a band-limited signal. The sampling density is high for large signal levels. (c) IF-TEM sampling by using burst signals with positive amplitudes. We observe that there are no samples when the signal is inactive, whereas a conventional ADC would sample during the entire time interval.

Finite-Rate-of-Innovation Signal Reconstruction From Integrated and Fire Time-Encoding Machine Samples

To determine finite-rate-of-innovation (FRI) parameters from integrated and fire time-encoding machine (IF-TEM) samples, we assume that the FRI signal is filtered through a sum-of-sincs (SOS) kernel, as in (3), and the output signal $y(t)$ [see (4)] is sampled using an IF-TEM. Let the time encodings be $\{t_n\}_{n=1}^{N}$. Using (15), we compute the following amplitude measurements from time encodings: $y_n = \kappa\Delta - b(t_n - t_{n-1}) = \int_{t=t_{n-1}}^{t_n} y(t)\,\mathrm{d}t$, $n = 1,\ldots,N-1$. From the trigonometric polynomial form of $y(t)$ in (4), the Fourier samples are related to the measurements as

$$y_n = \sum_{k\in\{-K,\ldots,K\}\setminus 0} F(k\omega_0)\frac{(e^{jk\omega_0 t_{n+1}} - e^{jk\omega_0 t_n})}{jk\omega_0} + F(0)(t_{n+1} - t_n),\ n = 1,\ldots,N-1 \qquad \text{(S6)}$$

where $K \geq L$. It was shown that the Fourier samples $\{F(k\omega_0)\}_{k=K}^{K}$ are uniquely determined from the measurements $\{y_n\}_{n=1}^{N-1}$ using (S6) if $N \geq 2K+2$ [10]. The condition $N \geq 2K+2$ can be satisfied by choosing the IF-TEM parameters as $\mathrm{FR}_{\min} > 2K + 1/t_{\max}$, where $t_{\max}$ represents the maximum time delays of the FRI signal. The latter condition is similar to that for reconstructing band-limited signals from IF-TEM samples, where it is required that $\mathrm{FR}_{\min}$ be greater than the Nyquist rate.

After the Fourier samples are obtained from the time encodings, the FRI parameters can be computed using either Prony's approach or other robust methods, as discussed previously.

comparators defines the system resolution, similar to conventional flash ADCs. Hence, the integrator power consumption is given as

$$P_{\text{INT}} = 96kT\alpha f_s \tag{18}$$

where αf_s is the switching or reset rate of the integrator. It is purposely written in terms of the sampling rate f_s of the conventional ADC (see Figure 11). The sampling activity factor α shows how the nonuniform switching rate of an integrator relates to the sampling frequency of conventional ADCs. For example, in the case when the average switching rate of an integrator approaches the conventional ADC sampling frequency f_s in the case of a fast-changing signal, as in Figure 10(b), α approaches or goes above a value of one. If the average sampling rate (switching rate) of an IF-TEM is much lower than that of the conventional ADC in the case of burst signals, with activity only in some time intervals [as in Figure 10(c)], then $\alpha \ll 1$, an important case for event-driven low-power data conversion systems. Our power analysis reflects these changes in the activity factor.

Overall, the sampling activity factor $\alpha > 0$ is a quantity that depends on the signal to be sampled and the reconstruction methods, as discussed in the following. The reset rate has a similar notion as the f_{FB} in the case of the modulo ADC discussed in the "Power Analysis of Modulo ADC" section. To compute the comparator's power consumption, we use (S2) with an assumption that the comparator has the same characteristics as the comparators in the flash ADC. Then, for $n = 1$, the comparator power is given as

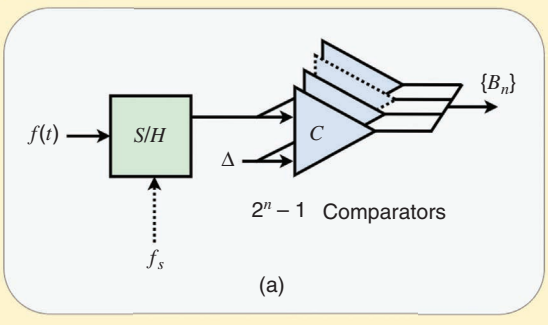
$$P_{C,\text{IF-TEM}} = 8 \ln 2 V_{\text{eff}} C_C \alpha f_s A. \tag{19}$$

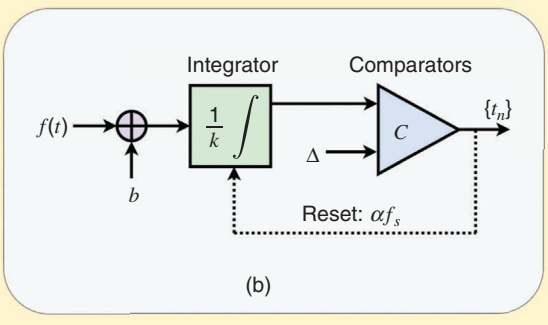
The total estimated power of the IF-TEM is

$$\begin{aligned} P_{\text{IF-TEM}} &= P_{\text{INT}} + P_{C,\text{IF-TEM}} \\ &= 96kT\alpha f_s + 8 \ln 2 V_{\text{eff}} C_C \alpha f_s A \\ &= \frac{\alpha}{2^{2n-2}} P_S + \frac{2\alpha}{(2^n - 1)n}((2^n - 1)P_C) \end{aligned} \tag{20}$$

where P_S and $(2^n - 1)P_C$ are the power requirements of the S/H and quantizer parts [see (S1)], respectively, in a conventional ADC. We assume that the comparators are the same for both the conventional ADC and the IF-TEM.

From (20), we note that for $\alpha < \max(2^{2n-2}, (2^n - 1)n)$, where $n > 1$, $P_{\text{IF-TEM}}$ is smaller than the power of a conventional ADC. The power saving is largely due to the fact that there is only a single comparator in the IF-TEM compared to the conventional flash ADC, where there are $2^n - 1$. Even if one uses a different quantizer than the flash-type one, the





	Conventional ADCs	IF-TEM
Sampling Frequency	f_s	αf_s
Resolution (Bits)	n	1
Sampling Power	$P_S = 24\ kT f_S\ 2^{2n}$	$96\ kT\ \alpha f_S$
Comparator Power	$P_C = 4n \ln 2\ V_{\text{eff}}\ C_C\ f_S\ A$	$8 \ln 2\ V_{\text{eff}} C_C\ \alpha f_S A$
Total Power	$P_S + (2^n - 1)\ P_C$	$\frac{\alpha}{2^{2n-2}} P_S + \frac{\alpha}{n} P_C$

(c)

FIGURE 11. An architecture and power consumption estimation comparison between (a) a conventional flash ADC (synchronous) and (b) an asynchronous IF-TEM, showing (c) the corresponding power savings for the latter system.

number of comparators can be reduced at the expense of other circuitry; still, the power saving of the IF-TEM can be reduced if $\alpha < 1$. Hence, in the aforementioned analysis, α plays a key role, and next, we discuss its dependency on the class of signals and reconstruction algorithm.

First, we consider band-limited signals whose Nyquist rate is f_{Nyq}, and hence, the conventional ADC operates at the minimum rate $f_s = f_{\text{Nyq}}$. For these signals, as discussed earlier, reconstruction from IF-TEM samples is possible if $\text{FR}_{\min} > f_{\text{Nyq}}$ [9]. If for a given signal's DR A, we choose IF-TEM parameters $\{b, \kappa, \Delta\}$ such that $\text{FR}_{\min} > f_{\text{Nyq}}$ is satisfied, then from (17), we know that the FR could be much higher than the Nyquist rate, specifically, $\alpha > (b + A/b - A) > 1$. This implies that the IF-TEM always fires even if the input signal's amplitude does not change significantly. This fact is also depicted in Figure 10(b). For band-limited signals, a large value of α above one reduces the effective power saving even if $\alpha < \max(2^{2n-2}, (2^n - 1)n)$.

On the other hand, signals that are not necessarily band limited but are bursty in nature, where the signal's amplitude is above a certain level only in a few intervals, are much more suited for sampling by using an IF-TEM. Assume that the reconstruction is not a sinc-based interpolation as in the Shannon–Nyquist framework but uses a local interpolation, such as a linear or a spline-based one. In such scenarios, $\text{FR}_{\min}$ can be set to zero, which implies that there are no firings when the signal is not active, and the signal is reconstructed, up to a given accuracy, from the time encodings in the active period. In this case, $\alpha < 1$. An example of such a burst signal, which is similar to an FRI signal, is in Figure 10(c), where the signal is active in certain time intervals and zero elsewhere. We assume that the signal is positive such that $0 \le f(t) \le A$, and hence, bias is not added; that is, $b = 0$. Then, for $\kappa = 1$ and a particular value of Δ, we note that there are no firings during the inactive period of the signal. This implies that the integrator and the comparator were not activated, i.e., they were in sleep mode, in those intervals. However, if a conventional ADC is used to sample such signals, then the integrator and comparator operate in both active and inactive modes and consume relatively higher power. Because of this reason, time encoding-based ADCs, including IF-TEMs, are preferable in event detection applications, such as biosignal monitoring in wearable devices, voice activity detection by voice-based virtual assistant platforms, and more. On another application front, event-based cameras are an emerging field, where it is shown that they have higher resolution and lower power consumption than conventional cameras.

Several integrated circuit implementations of level crossing-based systems are available [46]. However, there is very little work on IF-TEM-based ADCs. In [18], a hardware prototype of an IF-TEM ADC was presented, where the reconstruction of FRI signals from time encodings was demonstrated (see Figure 12). The authors showed that the FR is 10 times below the Nyquist rate of the signals.

While IF-TEMs offer energy efficiency, they exhibit certain limitations. A primary concern is oversampling, which occurs due to the requirement that the minimum FR must exceed the Nyquist rate or the threshold for a given signal class. This can lead to scenarios where the maximum FR significantly surpasses the minimum, particularly in regions of high signal amplitude, resulting in oversampling and elevated firing density, which can increase power consumption. Another issue stems from the integrator in IF-TEMs, which functions as a low-pass filter. This filtering attenuates high-frequency components of the input signal, potentially degrading the accuracy of signal reconstruction. Moreover, the introduction of bias in the firing process reduces the sensitivity of the firing times to the input signal, further impairing reconstruction fidelity.

On the other hand, level-crossing ADCs directly utilize the signal's samples and the times at which level crossings occur, without requiring an integrator. As previously mentioned, this can be implemented using multiple- or dual-comparator hardware architectures, where level crossings are encoded as "up" or "down" transitions [42], in contrast to the IF-TEM, which employs a single comparator. Since the signal samples itself, there is no risk of aliasing [47], and the framework is designed to reduce the sampling rate.

The level-crossing flash ADC structure can be modeled as a quantizer stage consisting of $(2^n - 1)$ analog comparators functioning as zero-crossing detectors. Various methods exist for reconstructing these nonuniform samples [47], which differ from the conventional Shannon–Nyquist reconstruction approach. Similar to

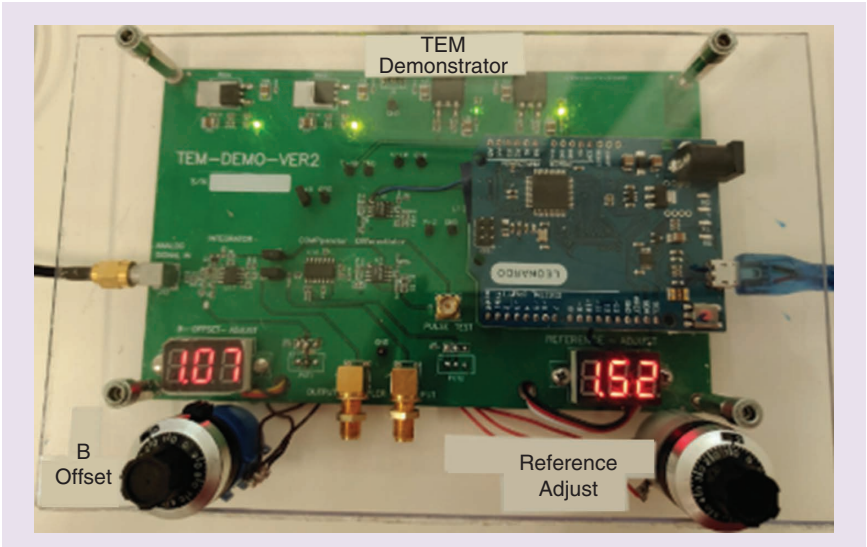


FIGURE 12. A hardware prototype of an IF-TEM sampler [18].

the IF-TEM, the zero-crossing rate of the system can be expressed as αf_s, where α represents a nonuniform sampling activity factor, indicating irregular sampling intervals. Consequently, the power consumption of the quantization stage can be estimated as αP_C, where P_C is the power consumption of the corresponding stage in a conventional flash ADC. However, additional circuitry is required for the reconstruction of nonuniform samples, which introduces a bottleneck to the system.

In the previous sampling frameworks, the focus was on reducing the sampling rate and the DR of the signal to reduce power consumption. In this section, we discuss methods to reduce the number of quantization bits by exploring the task at hand. For signal reconstruction with acceptable accuracy, samples should be encoded with a sufficiently large number of bits. However, in many applications, the task is not signal reconstruction but extracting some information from the analog signal [11]. For example, in a multiple-input, multiple-output (MIMO) communication system, it is necessary to estimate the channel, which is a low-dimensional task compared to underlying analog signal recovery. In such applications, task-based quantization is proposed, where by using analog combiners and joint optimization of an analog front end and digital back end, the number of quantization bits can be significantly reduced [11].

Theoretical framework of task-based quantizer

To understand the task-based low-bit quantization system, let us consider a discrete model in which we assume that the signals are already sampled [11]. The assumption helps us in focusing only on the quantization part. The general framework of task-based quantization is displayed in Figure 13(a), where the goal is to estimate a low-dimensional vector or task $\mathbf{s} \in \mathbb{R}^K$ from measurements $\mathbf{x} \in \mathbb{R}^N$, where $K < N$. The information $\mathbf{s}$ is statistically dependent on observations $\mathbf{x}$ via a conditional distribution $f_{\mathbf{x}|\mathbf{s}}$. For example, $\mathbf{x}$ represents directions of arrivals, and $\mathbf{y}$ is a snapshot of N sensors or antennas for the case of radio receivers. Instead of individually quantizing entries of $\mathbf{x}$ by using N scalar quantizers, the measurement $\mathbf{y}$ is projected to a low-dimensional space by using a combiner $h_a : \mathbb{R}^N \to \mathbb{R}^P$. Each component of the combiner $(h_a(\mathbf{x}))_p, 1 \le p \le P$ is independently quantized by a scalar quantizer $Q^1_{M_P}(\cdot)$ to get quantized measurements $Q^1_{M_P}((h_a(\mathbf{x}))_p), 1 \le p \le P$. Here, M_P represents the number of levels of each quantizer. The vector $\mathbf{s}$ is estimated from the quantized measurements as

$$\hat{\mathbf{s}} = h_d\left(Q^1_{M_p}((h_a(\mathbf{x}))_1), \ldots, Q^1_{M_p}((h_a(\mathbf{x}))_p)\right) \tag{21}$$

where $h_d(\cdot) : \mathcal{R}^p \longmapsto \mathcal{R}^k$ is an estimator. The aforementioned system is hardware limited by assuming that the number of

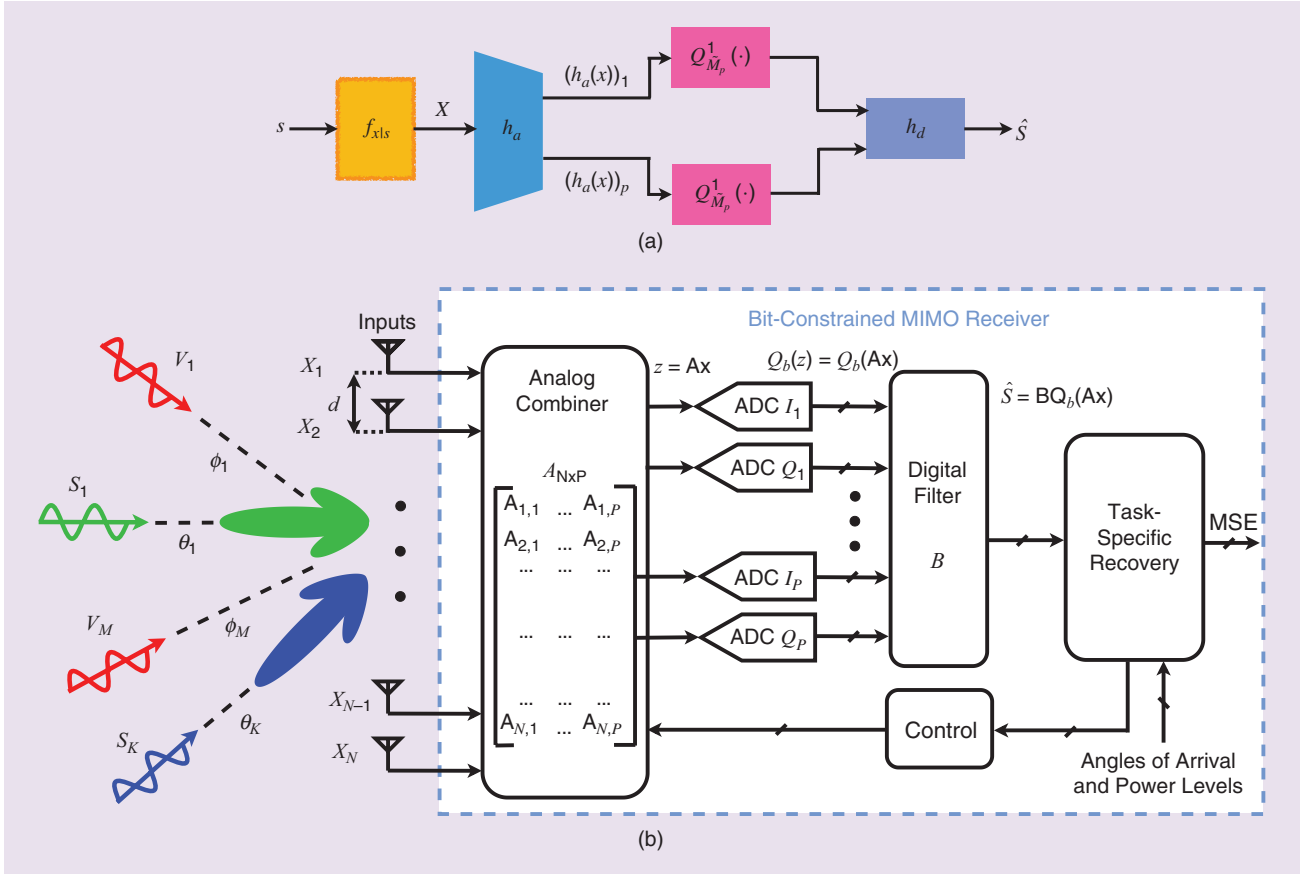


FIGURE 13. (a) A task-based quantizer. (b) A task-specific hybrid MIMO receiver system utilizing low-quantization-rate ADCs and a power-efficient analog combiner [23]. MSE: mean square error.

quantization levels available, M, is fixed. This implies that M_P should satisfy the inequality $M_P \leq M^{1/P}$.

The goal of a hardware-limited task-based system is to jointly optimize the combiner $h_a(\cdot)$, quantizer Q_{M_P}, and estimator $h_d(\cdot)$. The problem is intractable without making explicit assumptions about the stochastic model $f_{\mathbf{x}|\mathbf{s}}$. For example, one can consider a linear model $\mathbf{x} = \mathbf{A}\mathbf{s} + \mathbf{w}$, where $\mathbf{w}$ is noise [11]. Such models are common in many estimation tasks. Further, the combiner and estimator are assumed to be linear and represented by matrices. Within this linear setting, the authors of [11] derived expressions for the combiner matrix and estimator that minimize the mean square error (MSE) in the estimation of $\mathbf{s}$ for a fixed M. The results are also extended to the measurements related to $\mathbf{s}$ in a quadratic fashion [12]. In a nutshell, by reducing the dimension of the measurements from N to P, one can assign more bits during quantization when the overall number of bits is fixed. This improves the estimation accuracy.

Deep learning-based methods are also applied when the observations and unknowns, such as channel parameters, cannot be represented linearly or quadratically [48]. Further, at the application front, task-based methods are applied to massive MIMO communications for estimation of the underlying channel from the high-dimensional received signals [49].

Task-based ADC hardware

A hardware prototype for MIMO channel reduction with the task of estimating the underlying channel is presented in [19].

Task-Specific Multiple-Input, Multiple-Output Recovery Algorithm

Task-specific multiple-input, multiple-output receiver design constraints can be accounted for in the convex optimization framework by formulating a loss measure:

$$\mathcal{L}(\boldsymbol{A}) = \mathrm{MSE}(\boldsymbol{A}) + \gamma_I \mathrm{IntRej}(\boldsymbol{A}) + \gamma_S \| \boldsymbol{A} \|_{1,1}. \quad \text{(S7)}$$

Here, $\| \cdot \|_{1,1}$ is the entry-wise ℓ_1-norm operator, while $\gamma_I, \gamma_S \geq 0$ are regularization coefficients, balancing the contribution of the task recovery mean square error, spatial interferer rejection, and sparsity level of the analog combiner in the overall loss measure. In addition, although (S7) is expressed in the convex term, the final solution, accounting for the finite vector modulator resolution, is defined over a discrete domain space. The final objective is formulated as

$$\boldsymbol{A} = \underset{\boldsymbol{A} \in \mathcal{A}^{P \times N}}{\operatorname{argmin}} \mathcal{L}(\boldsymbol{A}). \quad \text{(S8)}$$

The recovery algorithm performs $k_{\max}$ rounds of a convex optimizer for minimizing $\mathcal{L}(\boldsymbol{A})$ over $\mathcal{C}^{P \times N}$, with periodic projections onto the discrete $\mathcal{A}$. Algorithm 1 summarizes the design procedure.

One of the main goals of low-bit quantization using a task-based (task-specific) framework is to reduce the overall system's power consumption. Implications of task-based receiver system design are considered in detail in this section. First of all, as previously mentioned, the power consumption of the ADCs is directly proportional to the number of bits, as suggested by Walden's FOM [2].

The task-based framework discussed earlier was shown to reduce the quantization rate quite significantly (two to six times). However, additional analog processing is required for such systems, resulting in increased analog hardware complexity that is directly tied to power consumption, which is especially critical in MIMO receivers since the analog processing overhead is proportional to the hardware processing channels. In fact, power efficiency, hardware complexity, and signal recovery accuracy are critical performance tradeoffs for MIMO modern communication systems.

In [23], energy-efficient analog processing together with low-quantization ADCs and task-specific processing for MIMO receivers was developed. Recent MIMO developments particularly focus on communication in congested environments, where both desired signals and undesired jammers arrive from various directions at the receiver.

Generally, the signal model at the MIMO receiver can be described, as vector $\boldsymbol{x}$ is an input observation vector consisting of a linear combination of K desired signals (tasks) arriving from corresponding angles θ_K. In addition, a set of M undesired signals (spatial blockers) arrives from respective angles ϕ_K, as demonstrated in Figure 13(b). Input observation signals are first processed in the analog combiner $\boldsymbol{A}$, performing linear matrix multiplication with signal dimensionality reduction, similar to the $h_a(\cdot)$ combiner in the task-based quantization system discussed earlier [Figure 13(a)]. The output of the analog combiner is quantized using low-resolution ADCs [modeled as a scalar quantizer $Q_b(\cdot)$] and processed in the digital domain using matrix $\boldsymbol{B}$, similar to estimator $h_d(\cdot)$, obtaining desired signal (task) estimate $\hat{\boldsymbol{s}} = \boldsymbol{B}\boldsymbol{Q}_b(\boldsymbol{A}\boldsymbol{x})$.

Several hardware design considerations were accounted for in the solution algorithm. First, the system targets low-bit ADC task recovery without compromising recovery accuracy. Second, while the MSE focuses on task recovery, a spatial blocker impression in the analog domain before analog-to-digital conversion is embedded to avoid receiver desensitization and an increased DR requirement of the ADCs. Finally, the system targets a highly power-efficient operation of the

Algorithm 1: Analog combiner setting

Data: Fix $\boldsymbol{A}^{(0)}$
for $k = 1, 2, \ldots, k_{\max}$ **do**
  Update $\boldsymbol{A}^{(k)} \leftarrow O_{\mathcal{L}}(\boldsymbol{A}^{(k-1)})$
  if $\mathrm{mod}(k, k_{\mathrm{proj}}) = 0$ **then**
    Project via $\boldsymbol{A}^{(k)} \leftarrow \mathcal{P}_{\mathcal{A}}(\boldsymbol{A}^{(k)})$
  end
end
Output: Analog combiner $\boldsymbol{A}^{(k_{\max})}$.

analog combiner to reduce the overhead from analog preprocessing. The details of the task-specific MIMO optimization algorithm are provided in "Task-Specific Multiple-Input, Multiple-Output Recovery Algorithm."

The power consumption of a MIMO receiver can be estimated from the power consumption of the subblocks of the system. Conventional MIMO receiver hardware, shown in Figure 14(a), consists of an analog signal acquisition block, such as low-noise amplifiers, variable-gain amplifiers, and phase shifters that perform some form of signal processing in the analog domain, for example, for beamforming. For analysis simplicity, we consider an implementation using vector modulators (VMs), circuit components that apply a simultaneous complex gain and phase shift on the input signal. The next crucial component is a mixer, which performs signal downconversion from carrier to baseband frequencies. Signals are then amplified using baseband amplifiers and quantized using ADCs. With N input signals and N output streams, conventional MIMO system power consumption is expressed as

$$P_{\text{conventional MIMO}} = NP_{\text{VM}} + NP_{\text{MIX}} + 2NP_{\text{BB}} + 2NP_{\text{ADC}} \quad (22)$$

where P_{VM} is the power consumed by the VM, P_{MIX} is the downconversion mixer consumption, and P_{BB} and P_{ADC} are the baseband amplifier and ADC power consumption, respectively, each doubled to account for the quadrature I and Q paths.

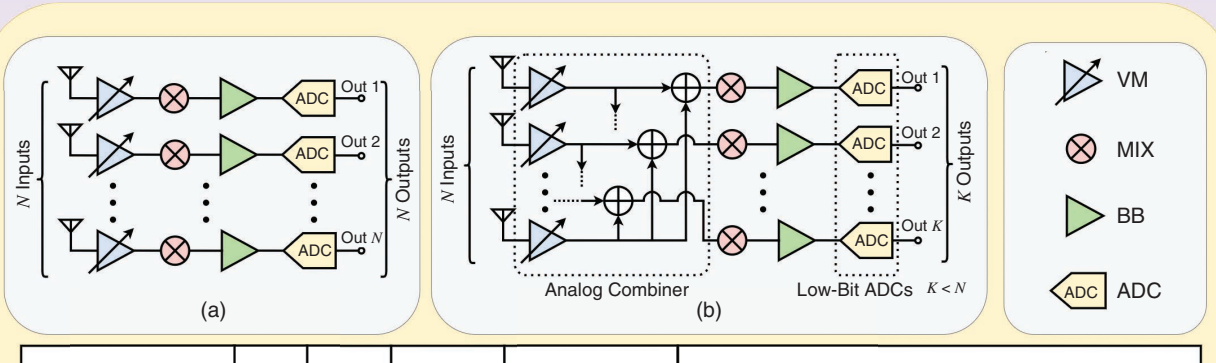
The task-specific MIMO receiver, on the other hand, first processes input signals in the analog combiner, which performs analog preprocessing with dimensionality reduction. For a system with N input signals and K output streams, where $K < N$, the number of required VMs is $N \times K$. However, due to the lower number of output signals, only K baseband processing chains are needed. In addition to that, one has to consider optimal analog preprocessing circuit design such that the power overhead from the prequantizing analog combiner will not exceed the power savings enabled by the low quantization rate. Overall analog combiner power consumption depends on the number of active VM elements in $\boldsymbol{A}$ and individual VM power consumption, which is proportional to the VM resolution. By utilizing sparsification of $\boldsymbol{A}$ (zeroing particular elements of matrix $\boldsymbol{A}$), implemented as keeping the corresponding VM in sleep mode, and incorporating fine and coarsely quantized VMs, additional power savings in the analog combiner can be achieved. Hardware nonidealities, in this case, are accounted for in the back-end convex optimization algorithm.

The resulting system power consumption expression is

$$P_{\text{task-specific MIMO}} = \gamma_{\text{SP}} NKP_{\text{VM}} + KP_{\text{MIX}} + 2KP_{\text{BB}} + 2KP_{\text{ADC}} \quad (23)$$

Here, γ_{SP} is the analog combiner sparsity coefficient; $\gamma_{\text{SP}} = 1$ denotes a nonsparse $\boldsymbol{A}$, while a practical value of $\gamma_{\text{SP}} = 0.75$, which corresponds to 25% sparsity, is used in the system. Figure 14(b) features a task-specific MIMO receiver and system parameters with power consumption estimation expressions. It is important to note that task-specific MIMO incorporates additional power savings from low-resolution VMs and ADCs.

The proposed solution implementation was simulated in MATLAB in [23]. The numerical results in [23] show that the quantization rate can be reduced by a factor of four compared to conventional fully digital MIMO for the same accuracy. In addition, power consumption estimation based on state-of-the-art integrated components shows that a more than 58% power reduction can be achieved compared to the task-agnostic solution by incorporating the sparsity of the analog combiner, variable-resolution VMs, and low-resolution ADCs while



	Inputs	Outputs	VMs	MIXs/BBs/ADCs	Total System Power Consumption
Conventional MIMO	N	N	N	N	$N P_{\text{VM}} + N P_{\text{MIX}} + 2N P_{\text{BB}} + 2N P_{\text{ADC}}$
Task-Specific MIMO	N	K	$N K$	K	$\gamma_{\text{SP}} N K P_{\text{VM}} + K P_{\text{MIX}} + 2K P_{\text{BB}} + 2K P_{\text{ADC}}$

(c)

FIGURE 14. An architecture and power consumption estimation comparison between (a) conventional MIMO and (b) task-specific MIMO. (c) Power comparison of the conventional MIMO and task-specific MIMO. VM: vector modulator; MIX: mixer; BB: baseband amplifier.

suppressing interferers by more than 36 dB [23]. An integrated circuit implementation of this work was demonstrated in [50], showing successful signal recovery in hardware with 2-bit ADC quantization in a MIMO communication scenario.

Regarding the ADC power consumption estimation, we recall from the discussion above that typical flash ADC power is estimated as $P_{SH} + (2^n - 1)P_{CADC}$, where n is the number of bits. Although the theoretical power saving gain should be exponentially proportional to the reduction of the number of bits, practical ADC implementations exhibit power consumption overhead coming from other peripheral circuits (digital processing and the biasing network), especially at a low resolution, when the consumption of those subblocks becomes more dominant. This creates a power consumption floor for low-resolution ADCs, as demonstrated in the ADC performance survey [21].

Conclusions

Low-power ADCs are key for emerging applications. In this article, we discussed four approaches that can be applied to reduce the power consumption of ADCs. Among these techniques, three directly reduce power by reducing the sampling rate, DR, and resolution of an ADC, whereas the fourth method relies on a time-based discrete representation of the signal. Any two or more of these methods can be combined to make the sampling process even more power efficient. A common feature of the four frameworks is to have a preprocessing analog front end, a low-power ADC, and a digital signal processor. For these four frameworks, we discussed power consumption and hardware prototypes that are developed in our labs. These power-efficient ADCs play a crucial role in designing compact portable medical and communication devices.

Acknowledgment

We would like to acknowledge several authors' publications and research works that are relevant to this review. We could not cite them due to a strict restriction on the number of references. This work is partially supported by Semiconductor Research Corporation Task 3160.027, through the University of Texas at Dallas' Texas Analog Center of Excellence.

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