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*e*Sampling: Energy harvesting ADCs☆

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ABSTRACT

The power consumption of analog-to-digital converters (ADCs) imposes a major challenge in power-limited systems. A common ADC architecture is based on sample-and-hold (S/H) circuits, where the analog signal is tracked only for a fraction of the sampling period. In this paper, we propose *eSampling ADCs*, which extend the structure of S/H ADCs without altering the conversion procedure, while allowing energy harvesting from the analog signal during the time periods where the signal is not tracked. The amount of energy harvested can be increased by reducing the sampling rate. We analyze the tradeoff between signal recovery and the energy harvested, and provide guidelines for setting the sampling rate in light of accuracy and energy constraints. Further, the feasibility of *e*Sampling ADCs is validated by simulating a circuit-level design of an 8-bit *e*Sampling ADC in standard CMOS 65 nm technology. The implemented ADC operates at a supply voltage of 1V and sampling rate of 40 MHz. Our analysis shows that *e*Sampling ADCs are able to perfectly recover (up to the distortion induced by quantization) the acquired bandlimited analog signals, while harvesting a significant fraction of the power consumed in acquisition. The experiment demonstrates that *e*Sampling ADC can harvest 21.5% of the energy it spends during analog-to-digital conversion, without affecting the accuracy in reconstructing the analog signal. Finally, we establish the effectiveness of the proposed system by powering a commonly used on-system circuitry operational amplifier (op-amp) entirely using the harvested energy.

1. Introduction

Physical signals are analog in nature, taking values in continuous sets over a continuous time interval. In order to process and extract information from such signals using digital hardware, they must be accurately represented in digital form. Analog-to-digital converters (ADCs) thus play an important role in digital signal processing systems [2]. ADCs are typically a major source of energy consumption, as their power dissipation grows with the sampling rate and quantization resolution, and thus their ability to accurately represent the acquired signal is typically limited by the available power [3]. Nowadays, ADCs are utilized in a multitude of energy-limited systems, including communication devices [4], wireless sensors [5], and medically implanted devices [6]. Therefore, there is a growing need for ADCs capable of reliably acquiring signals while consuming low power.

The existing strategies proposed in the literature to facilitate energy-efficient acquisition of analog signal can be divided into those taking a signal processing approach, and techniques focusing on circuit level design. Signal processing approaches typically aim for allowing the ADC to operate at reduced sampling rate and quantization resolution by accounting for how the acquired signal is processed and prior information on the signal itself [5,7–10]. Additionally, in scenarios where the signal is acquired for some task, i.e., to recover some underlying information, it was recently shown that the desired information could be accurately recovered from the output of low-resolution ADCs by properly designing the acquisition system [11–15]. An alternative signal processing oriented method which does not limit the rate and resolution of ADC is based on acquiring a portion of the analog signal to be processed while utilizing the remaining part for energy harvesting. This strategy,

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typically studied in the context of communication receivers as simultaneous wireless information and power transfer (SWIPT), considers time or power splitting of the analog signal [16–19]. However, it induces inevitable loss on the system performance as only a portion of the signal is converted into a digital representation. These aforementioned signal processing methods typically focus on the signal model and the task for which it is acquired, without accounting for the ADC circuitry.

Circuit level methods rely on the hardware architecture of ADC devices. This approach generally considers designing energy-efficient ADC circuitry, capable of operating with reduced power consumption by reducing the circuit power supply [6] and/or limiting the operating frequency [20]. An alternative technique is to modify the circuit components in existing ADC architectures and combine various designs in the acquisition, such as sample-and-hold (S/H) ADCs, flash ADCs, sigma-delta ADCs, and time-interleaved ADCs, to improve their energy efficiency, see, e.g., [21–24]. Such circuit-oriented designs which focus on the hardware aspects of acquisition, do not account for the model of the analog signal and the task for which it is acquired.

A popular power efficient ADC is the S/H based successive approximation register (SAR) architecture, which is capable of operating at high resolution and a small form factor with relatively low power consumption [25]. The power consumption of SAR ADCs can be further reduced by incorporating energy-efficient switching schemes, as proposed in [26,27]. In S/H architectures, the circuit used to sample the input analog signal consists of two phases, *acquisition phase* and *hold phase* in each sampling period. In the acquisition phase, the S/H circuit tracks the input analog signal. The sampled value captured in the acquisition phase is then converted into digital form, i.e., a sequence of bits, during hold phase. Therefore, during the sampling process of S/H ADCs, the input signal is processed only for a fraction of the overall sampling period (acquisition phase) and is neglected/discarded for the remaining time interval (hold phase) [28,29]. The fact that the signal is not accessed in a dominant portion of the sampling period, motivates the extension of S/H ADCs, and particularly S/H SAR ADCs, to continuously utilize the analog signal in order to harvest energy which is comparable to the amount of energy consumed during acquisition [1].

In this work, we combine signal processing tools with circuit level methods to propose an *e*Sampling ADC, which harvests energy from the acquired signal while converting it into a digital representation. The eSampling ADC builds upon the S/H ADC architecture, being a popular family of ADC circuits which naturally extends to include energy harvesting capabilities in its acquisition flow. In the resulting architecture, the signal is harvested during hold phase, i.e., when it is not utilized in conventional S/H ADCs. This operation allows *e*Sampling ADCs to harvest energy from the sampled signal without altering the conversion procedure. Our analysis of *e*Sampling ADCs formulates the theoretical foundations for joint acquisition and energy harvesting, and generalizes the experimental results of our previous work [30], which demonstrated that energy harvesting can be combined with sensing circuits. As opposed to SWIPT systems, in which the overall operation of the system is modified to allow energy harvesting while conventional ideal ADCs are assumed [19], *e*Sampling exploits an inherent property of ADC devices to harvest energy as a natural byproduct of their hardware architecture. This makes *e*Sampling an attractive technology which can be easily incorporated into existing devices.

Our theoretical study of *e*Sampling ADCs analyzes its potential in terms of the ability to harvest energy while maintaining a desired accuracy of signal reconstruction. To that aim, we focus on the acquisition of stationary random processes and characterize the resulting tradeoff between the ability to accurately reconstruct the signal from its samples and the energy harvested from it, referred to henceforth as the *energy-fidelity tradeoff*. Our analysis identifies how to set the sampling rate to optimize this tradeoff when operating under energy constraints or fidelity restrictions on the reconstruction. Our results allow to numerically characterize the maximal accuracy in which any signal can be *e*Sampled by harvesting a substantial portion of the energy consumed in acquisition, which is determined by the specific components comprising the ADC circuit. We show that *e*Sampling ADCs operating with a typical set of ADC parameters are capable of fully reconstructing signals of various power spectral density (PSD) profiles with negligible distortion, while harvesting energy from the analog signal.

We then proceed to illustrate the hardware feasibility of such a device. To that aim, we design the circuitry of an *e*Sampling 8-bit SAR ADC which samples at 40 MHz on 65 nm complementary metal oxide semiconductor (CMOS) technology, and provide guidelines for setting its parameters to achieve a desired amount of harvested energy. The experimental evaluation of the *e*Sampling SAR ADC circuit, carried out on the Cadence Virtuoso platform, shows that the amount of energy harvested during the conversion procedure is sufficient to drive important on-chip components such as operational amplifiers. This is achieved without affecting signal reconstruction accuracy when acquiring a bandlimited signal while satisfying the Nyquist condition. Our experiment indicates that the theoretical potential of *e*Sampling can be translated into an actual ADC circuit, which accurately acquires analog signals while harvesting non-negligible amounts of power.

The rest of this paper is organized as follows: In Section 2, we present our *e*Sampling system model. Section 3 analyzes the associated energy-fidelity tradeoff. The circuit-level design and its simulations are presented in Section 4. Finally, Section 5 provides concluding remarks.

2. System model

In this section, we present a high-level description of *e*Sampling. We begin by briefly reviewing S/H-based SAR ADCs and their associated energy consumption in Section 2.1. Then, we present how S/H ADCs can be extended into *e*Sampling ADCs which harvest energy in addition to signal acquisition in Section 2.2.

2.1. Sample-and-hold ADC model

2.1.1. High-level description

S/H is a common ADC architecture. Such ADCs acquire each sample in two phases, determined by a switch S, as illustrated in Fig. 1. In the acquisition phase, the signal is connected to a capacitor C_{h}, referred to as a holding capacitor, which is charged to the input analog voltage, as depicted in Fig. 1(a). The time required by the holding capacitor to charge to the input voltage, which dictates the acquisition time, is given by [25]

$$T_{\mathrm{aq}} = \alpha_\tau R_{\mathrm{on}} C_{\mathrm{h}}, \tag{1}$$

where R_{on} is the on-resistance of the switch S, and α_τ is the number of time constants, i.e., $R_{\mathrm{on}}C_{\mathrm{h}}$ required for the capacitor to be fully charged.

Once the acquisition phase is over, the hold phase begins, in which the discrete sample, i.e., the voltage stored in the holding capacitor, is quantized into digital bits. During hold phase, whose duration is denoted by T_{h}, the input signal is disconnected from the S/H circuit and C_{h} holds the acquired voltage to accomplish successful conversion of the acquired sample into digital bits as illustrated in Fig. 1(b). Both T_{h} and C_{h}, must be set to allow the quantization circuit of the ADC to complete the conversion.

When the quantizer is based on SAR logic, the overall architecture is referred to as a SAR ADC. An n-bit SAR ADC consists of a comparator, digital-to-analog converter (DAC), and a SAR logical circuit which successively refines the digital representation. To allow successful quantization into n bits, the hold time required to quantize each sample must satisfy [29]

$$T_{\mathrm{h}} \geq n\alpha_\tau R_{\mathrm{q}} C_{\mathrm{h}}, \tag{2}$$

where R_{q} is the equivalent resistance of the quantizer binary scale switches. Therefore, the sampling period, i.e., the duration of acquiring a single sample, is lower bounded by the following expression

$$T_{\mathrm{s}} = T_{\mathrm{aq}} + T_{\mathrm{h}} \geq (R_{\mathrm{on}} + nR_{\mathrm{q}})\alpha_\tau C_{\mathrm{h}}. \tag{3}$$

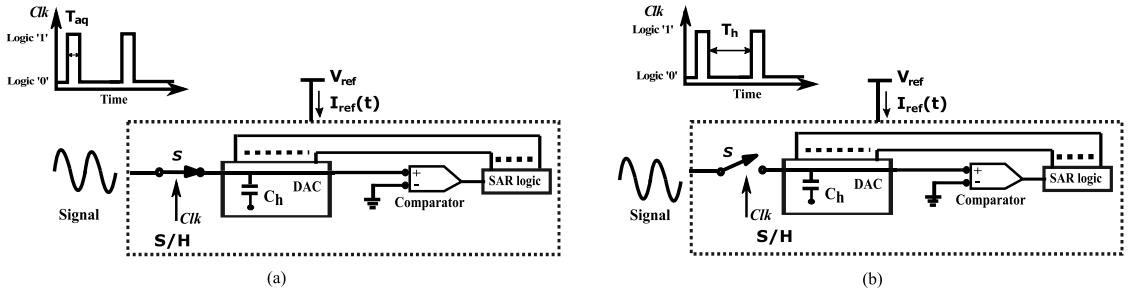

Fig. 1. S/H SAR ADC illustration: (a) acquisition phase (b) hold phase.

In S/H SAR ADCs, the on-resistance of the switch R_{on} is commonly not larger than the resistance of the quantizer binary scale switches R_{q}. Thus from (1) and (2), it is evident that T_{h} is typically much larger than T_{aq}, particularly when using high resolution quantizers, e.g., ADCs with $n \geq 8$ bits. Hence, the input signal, which is tracked only during the acquisition phase, is discarded during most of the sampling period.

2.1.2. Energy consumption

The energy consumption of a circuit is typically a function of the time duration it is active, and the amount of power drawn from the supply, denoted here by V_{ref}. As T_{h} is typically much larger than T_{aq}, most of the energy required by S/H SAR ADCs is consumed during hold phase [26,29].

In particular, the only energy consumed during acquisition phase, denoted E_{aq}, is that needed to toggle the sampling switch S. In contrast, the energy consumption during hold phase, denoted E_{hold}, is comprised of the energy used by each of the components taking part in the quantization:

$$E_{\text{hold}} = E_{\text{DAC}} + E_{\text{c}} + E_{\text{sl}}, \tag{4}$$

where E_{DAC}, E_{c}, and E_{sl} are the energy consumption of the DAC array, comparator, and SAR logic, respectively. Consequently, E_{hold} effectively represents the power consumed per sample by S/H SAR ADCs [26,29]. We elaborate on the quantities in (4), which are dictated by the specific circuit parameters used, in Section 4 where a concrete circuit-level design is discussed. Here, we note that E_{hold} typically takes the form of a second-order polynomial in the reference voltage, which is equal to the supply voltage, i.e., V_{ref}, and is given by [31]

$$E_{\text{hold}} = a_1(n)V_{\text{ref}} + a_2(n)V_{\text{ref}}^2. \tag{5}$$

The coefficients $a_1(n)$ and $a_2(n)$ in (5) are positive constants determined by the number of bits n and the quantization circuit parameters, and can grow dramatically with n. This makes energy consumption a major bottleneck of high resolution ADCs, motivating the proposed *e*Sampling architecture detailed next.

2.2. *e*Sampling ADC architecture

As mentioned above, during hold phase, the capacitor C_{h} holds the acquired voltage sample, which is converted into a set of digital bits. In this phase, the input signal is disconnected from the circuit by the switch S, and hence we propose to harvest the input signal energy by connecting it to an energy harvesting circuit, as illustrated in Fig. 2. Henceforth, the proposed architecture is referred to as an *e*Sampling ADC.

As depicted in Fig. 2, the energy harvesting capability is enabled by passing the signal observed during hold time through a conditioning circuit, whose output is used to charge an energy harvesting capacitor C_{EH} to a voltage level V_{EH}. The energy of this analog signal is harvested by this dedicated circuitry. This circuit can be designed using passive elements, as we do in our proof-of-concept detailed in Section 4. Hence, no external power supply is required [32]. The purpose of the signal conditioning circuit used in energy harvesting devices is to facilitate the storage of the energy of the signal in the capacitor C_{EH} [33–35]. For instance, a rectifier can act as a signal conditioning circuit, reducing fluctuations in the amount of energy harvested in the presence of alternating signals. Similarly, voltage regulator circuits and DC-DC step up converters can also enhance the overall efficiency of the energy harvesting system [36]. The common measure for the quality of an energy harvesting circuit is the efficiency parameter $\eta \in [0, 1]$, representing the fraction of the energy of the input signal that is harvested. Finally, to connect the input signal to the quantization circuit during acquisition time and to the energy harvesting circuit during hold time, the sampling switch S is replaced by a two-way switch $\tilde{S}$. A possible circuit design of such a two-way switch is detailed in Section 4.

The amount of energy consumed in acquisition phase given in (5) is dictated by the design parameters of the circuitry, which also affect the sampling rate via (3). In particular, the sampling duration is the sum of the acquisition time T_{aq} and the hold time T_{h}. Further, the amount of time during which energy is harvested from the input signal per sampling period is at most T_{h}. Recalling that typically $T_{\text{h}} \gg T_{\text{aq}}$, a significant portion of the sampling interval can be allocated for harvesting energy from the input signal. Since energy is only harvested during hold time, in which conventional S/H ADCs do not utilize the analog signal, the ability to harvest energy in *e*Sampling ADCs *does not affect the acquisition operation*. Specifically, for a given sampling rate, *e*Sampling ADCs implement the same conversion mapping as standard S/H ADCs operating at the same rate. Nonetheless, *e*Sampling provides the ability to trade acquisition accuracy for harvesting more energy. This follows since increasing the sampling interval allows *e*Sampling ADCs to dedicate more time to energy harvesting, possibly at the cost of degrading the accuracy in reconstructing the signal from its digital representation.

The goal of our analysis of *e*Sampling ADCs presented in the following section is to quantify the theoretical potential benefits of such an architecture, which is capable of simultaneously acquiring analog signals into a digital form while harvesting their energy. Both the amount of energy consumed in conversion and that harvested in *e*Sampling are determined by the specific circuitry, encapsulated in (5) and the energy efficiency parameter η, respectively. Therefore, in our analysis we fix the circuit parameters, e.g., $a_1(n)$, $a_2(n)$, η, and express how the accuracy in reconstruction and the amount of energy harvested vary as the sampling interval changes. We are particularly interested in (1) characterizing the amount of energy harvested in the regime in which the distortion induced by S/H conversion is negligible, e.g., Nyquist rate sampling of bandlimited signals; and (2) the amount of distortion induced when *e*Sampling ADCs operate at a regime where they are harvest at least as much energy as they consume.

3. *e*Sampling ADC analysis

In this section, we analyze the capabilities of the proposed *e*Sampling ADC in terms of the amount of energy one can harvest while meeting a given level of reconstruction accuracy, as well as

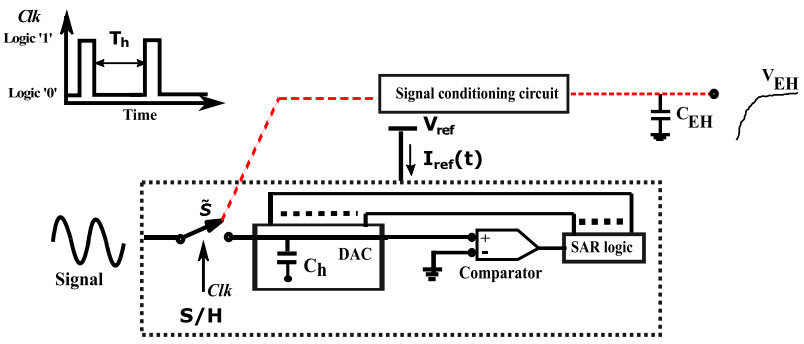

Fig. 2. Proposed *e*Sampling ADC system model.

the achievable accuracy for harvesting a desired amount of energy. The interplay between these key performance measures is determined by the selection of the sampling rate, as we show in the following. We begin by formulating the signal model under which our analysis is carried out, and the corresponding problem of characterizing the associated energy-fidelity tradeoff, which arises from the *e*Sampling ADC paradigm in Section 3.1. For tractability, our analysis focuses on stationary signals, and non-stationary signals are assumed bandlimited. This results in a generic and rigorous analysis, which in turn does not restrict the applicability of the eSampling ADC with different signal models. Then, we derive the achieved normalized mean-squared error (NMSE) under the considered model in Section 3.2. The NMSE is used to characterize the energy-fidelity tradeoff in Section 3.3, and to obtain as a special case the maximal amount of energy which can be harvested when sampling a bandlimited signal at a rate satisfying the Nyquist condition, i.e., allowing perfect recovery. We demonstrate a few examples of energy-fidelity tradeoff curves for signals with different spectral profiles in Section 3.4. Finally, we discuss the pros and cons of *e*Sampling ADC in light of our analysis in Section 3.5.

3.1. Problem formulation

The *e*Sampling ADC detailed in Section 2.2 harvests energy during hold phase. This implies that more energy can be harvested by increasing the hold time, which in turn increases the sampling period, potentially degrading the ability to reconstruct the signal from its samples. Therefore, to unveil the potential of *e*Sampling ADCs, we first wish to analyze the fundamental tradeoff between the amount of energy harvested in *e*Sampling and the resulting fidelity in signal reconstruction. We are particularly interested in: (1) Quantifying the maximum amount of energy that could be harvested when acquiring bandlimited signals at the Nyquist rate, i.e., without compromising the signal reconstruction accuracy; and (2) Characterizing the achievable NMSE when the ADC harvests at least as much power as it consumes.

In the analysis carried out in this section we consider a stochastic input signal $x(t)$ modeled as a zero-mean wide sense stationary (WSS) process, with variance σ_x^2, and PSD $S_x(f)$. The signal $x(t)$ is sampled uniformly with sampling interval T_s, resulting in the discrete-time signal $x(kT_s)$, $k \in \mathcal{Z}$, where $\mathcal{Z}$ is the set of integers. The sampled series is quantized with n bits per sample into the digital sequence $\tilde{x}(kT_s)$. The digital representation is utilized to recover the analog signal $x(t)$ using a linear reconstruction filter $G(t)$, which is designed to minimize the NMSE between $x(t)$ and the recovered signal $\hat{x}(t)$ as in [10,37]. The reconstructed signal is

$$\hat{x}(t) = \sum_{k\in\mathcal{Z}} G(t - kT_s)\tilde{x}(kT_s). \tag{6}$$

The overall system is illustrated in Fig. 3.

The NMSE in reconstructing $x(t)$ from $\hat{x}(t)$ is given by

$$\zeta = \frac{1}{\sigma_x^2 T_s}\int_0^{T_s} \mathbb{E}\{|x(t) - \hat{x}(t)|^2\}dt, \tag{7}$$

where $\mathbb{E}\{\cdot\}$ is the stochastic expectation. The amount of expected energy harvested per sampling period is given by

$$E_h = \eta\frac{1}{R_h}\int_{T_{aq}}^{T_s} \mathbb{E}\{|x(t)|^2\}dt = \frac{\eta}{R_h}T_h\sigma_x^2, \tag{8}$$

where η and R_h are the efficiency and the resistance of the energy harvesting circuit, respectively. As mentioned above, the energy harvesting circuit is comprised of passive elements, and does not require an external power source. Therefore, the overall energy consumption per sample using the proposed *e*Sampling ADC is $E_{aq} + E_{hold} - E_h$, as illustrated in Fig. 3. Recall that the overall energy consumption is typically dominated by the energy used during hold phase, i.e., $E_{aq} \ll E_{hold}$, and hence the ratio of the amount of energy harvested to the energy consumption per sample can be approximated as $E_{ratio} = \frac{E_h}{E_{hold}}$. The value of E_{hold} is dictated by the power supply voltage V_{ref} and the number of quantization bits n, as well as the SAR architecture and circuit parameters, as we show for our design detailed in Section 4.

In the following subsections, we study the fundamental tradeoff between the NMSE in the reconstruction, and the portion of the energy consumed in analog-to-digital conversion to that harvested by *e*Sampling, referred to as the *energy-fidelity tradeoff*. To trade energy efficiency for fidelity, we modify the sampling rate for a fixed quantization resolution n and fixed acquisition time T_{aq}. The reconstruction accuracy can be improved by increasing the sampling rate, however *e*Sampling ADC will harvest less energy, leading to an inherent tradeoff between these parameters. We focus on ADCs operating with relatively high resolution, where energy consumption constitutes a major challenge. Our analysis sheds light on the potential of joint acquisition and energy harvesting. For example, it quantifies the minimal recovery NMSE which allows a fixed n-bit ADC to operate at zero power, i.e., $E_{ratio} = 0$ dB. Alternatively, it allows identifying the quantization resolution n for which the *e*Sampling ADC can sample a bandlimited signal at the Nyquist condition and operate at minimum E_{ratio}. Finally, the characterization of the energy-fidelity tradeoff allows computing the maximal amount of energy which can be harvested for an allowed level of reconstruction accuracy for both bandlimited and non-bandlimited signals, as a function of the circuit parameters.

3.2. Reconstruction NMSE

In general, the NMSE depends on both the sampling rate as well as the quantization resolution [15]. Since we focus on relatively high rate quantization, the NMSE due to quantization is well-approximated by the 6 dB rule-of-thumb [38, Ch. 23], and is thus on the order of $10^{-0.6n}$ [25], resulting in a negligible contribution to the overall NMSE of less than roughly 10^{-5} for $n \geq 8$. Therefore, we focus on the NMSE between $x(t)$ and $\hat{x}(t)$ due to sampling alone, as expressed in the following theorem, derived in [37]:

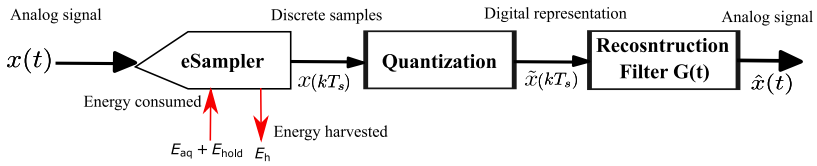

Fig. 3. Acquisition and reconstruction via *e*Sampling ADC illustration.

Theorem 1. *The minimal achievable NMSE in reconstructing a uniformly sampled WSS signal $x(t)$ with sampling frequency $f_s = 1/T_s$ using a linear reconstruction filter is*

$$\zeta(T_s) = 1 - \frac{1}{\sigma_x^2} \sum_{k\in\mathcal{Z}} \int_{-\frac{f_s}{2}}^{\frac{f_s}{2}} \frac{|S_x(f-kf_s)|^2}{\sum_{k'\in\mathcal{Z}} S_x(f-k'f_s)} df. \tag{9}$$

To achieve (9), the linear recovery filter $G(t)$ in (6) is set according to [10,37], i.e., its frequency response $\mathcal{F}(G)(f)$ is given by $\mathcal{F}(G)(f) = \frac{S_x(f)}{\sum_{k\in\mathcal{Z}} S_x(f-kf_s)}$, where $\mathcal{F}(\cdot)$ is the Fourier transform. This digital filter results in the minimal achievable NMSE between $x(t)$ and $\hat{x}(t)$. Theorem 1 generalizes the celebrated Shannon–Nyquist theorem, as stated in the following corollary:

Corollary 1. *When $x(t)$ is bandlimited and the sampling frequency satisfies the Nyquist condition, the NMSE is zero.*

Proof. If $x(t)$ is bandlimited, then there exists $f_m > 0$ such that $S_x(f) = 0$ for all $|f| > f_m$. When the sampling rate satisfies Nyquist condition, then $f_s \geq 2f_m$. Consequently, the summands in (9) are non-zero only at $k = k' = 0$, and hence

$$\begin{aligned}\zeta(1/f_s) &= 1 - \frac{1}{\sigma_x^2} \int_{-\frac{f_s}{2}}^{\frac{f_s}{2}} \frac{|S_x(f)|^2}{S_x(f)} df \\ &= 1 - \frac{1}{\sigma_x^2} \int_{-f_m}^{f_m} \frac{|S_x(f)|^2}{S_x(f)} df = 0,\end{aligned} \tag{10}$$

proving the corollary. ■

We next give an example of Theorem 1:

Example 1. Consider a bandlimited signal whose spectral support is $[-f_m, f_m]$ for some $f_m > 0$ with flat PSD. The obtained NMSE for such signals computed via Theorem 1 is

$$\zeta(1/f_s) = \begin{cases} 1 - \frac{f_s}{2f_m} & f_s \leq 2f_m, \\ 0 & \text{otherwise.} \end{cases} \tag{11}$$

Fig. 4 illustrates the recovery NMSE result of Theorem 1, showing which spectral portions of a signal with a flat PSD as in Example 1 are preserved by the NMSE minimizing reconstruction. In particular, Fig. 4 demonstrates how the complete spectrum is preserved when sampling above Nyquist rate, while sub-Nyquist sampling yields some recovery error due to aliased components. Fig. 4 also depicts the amount of energy harvested from the signal based on (8), showing that reduction in the sampling rate allows to harvest more energy in *e*Sampling at the cost of less accurate recovery, leading to the energy-fidelity tradeoff of *e*Sampling analyzed next.

3.3. Energy-fidelity tradeoff

In order to express the energy consumed in acquisition, we must first specify the voltage of the power supply V_{ref}. This value should be larger than the amplitude of the input signal with high probability to avoid overloading the ADC. Consequently, in the following we write the value of V_{ref} as some multiple $K > 1$ of the input standard deviation, i.e., the supply voltage is written as $V_{\text{ref}} = K\sigma_x$. This general formulation allows us to relate the reference voltage with the overload probability of the quantizer, since the overload probability satisfies $P(|x(t)| \geq V_{\text{ref}}) \leq K^{-2}$ by Chebyshev's inequality [11]. Therefore, the ratio between the expected energy harvested (8) and consumed (5) for *e*Sampling of a WSS signal can be written as

$$E_{\text{ratio}} = \frac{\frac{\eta}{R_h}(T_s - T_{aq})\sigma_x^2}{a_2(n)K^2\sigma_x^2 + a_1(n)K\sigma_x}. \tag{12}$$

Recall that for a fixed sampling interval, *e*Sampling ADCs implement the same conversion mapping as conventional S/H ADCs. Consequently, when one does not account for the distortion induced in quantization as we do here, WSS signals acquired by an *e*Sampling ADC operating with sampling interval T_s can be recovered with the NMSE $\zeta(T_s)$ stated in Theorem 1. We therefore use the expressions for the achievable NMSE (9) and the energy ratio (12) to characterize the energy-fidelity tradeoff of *e*Sampling.

Under the considered setting, we formulate how the recovery accuracy and the energy ratio behave as the sampling period T_s varies. Recalling that the acquisition time T_{aq} is determined by the ADC circuit parameters (1), modifying the sampling period is equivalent to tuning the hold time T_h. The energy-fidelity tradeoff of *e*Sampling is thus encapsulated in two complementary optimization problems: The first aims at finding the minimal achievable NMSE under a given energy constraint $\delta > 0$, i.e.,

$$\zeta^o(\delta) = \min_{T_s > T_{aq}} \zeta, \tag{13}$$

subject to $E_{\text{ratio}} \geq \delta$.

Setting $\delta = 0$ dB, implies that $E_{\text{hold}} = E_h$. Therefore, solving (13) with $\delta = 0$ dB leads to the minimal NMSE achievable by an *e*Sampling ADC which harvests at least as much energy as it consumes, i.e., when operating at zero power. A positive value of δ (in dB) implies an energy saving ADC which harvests more energy than its consumption per sample, namely, converting the signal only adds power to the system.

An alternative formulation seeks to maximize the energy harvested under a given fidelity constraint $\epsilon > 0$, i.e.,

$$E^o_{\text{ratio}}(\epsilon) = \max_{T_s > T_{aq}} E_{\text{ratio}}, \tag{14}$$

subject to $\zeta \leq \epsilon$.

For instance, consider a bandlimited signal. In such a case, one can achieve $\zeta = 0$ by *e*Sampling at the Nyquist rate, and harvest energy ratio $E^o_{\text{ratio}}(0)$, i.e., the maximal ratio of the harvested to energy to the consumed one when seeking ideal recovery. For non-bandlimited signals, approaching zero NMSE generally requires infinitesimally small sampling interval, which is not feasible due to the lower bound on T_s dictated by the ADC circuitry in (3). Consequently, when acquiring non-bandlimited signals (or extremely wideband signals), one would typically be more interested in evaluating (14) for some small yet feasible NMSE bound $\epsilon > 0$.

Problems (13)–(14) allow to characterize the energy-fidelity tradeoff, stated in the following theorem:

Theorem 2. *Let $T_h(\delta)$ be given by*

$$T_h(\delta) := \frac{\delta R_h}{\eta\sigma_x^2}\left(a_2(n)K^2\sigma_x^2 + a_1(n)K\sigma_x\right).$$

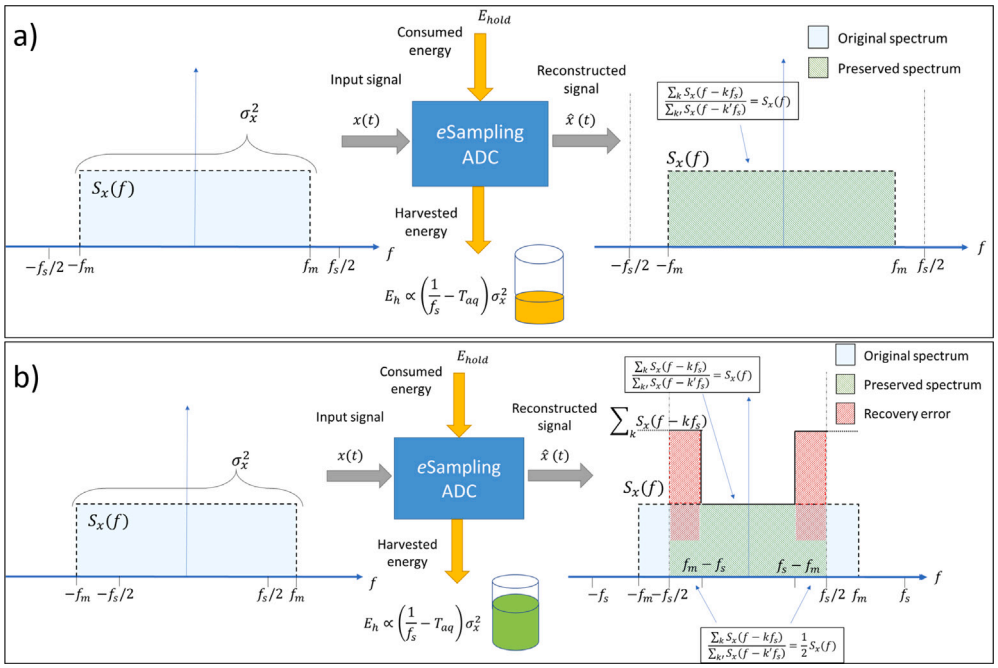

Fig. 4. Illustration of *e*Sampling of a signal with a flat PSD for: (a) Sampling at the Nyquist rate, while harvesting an amount of energy proportional to $T_h = 1/f_s - T_{aq}$; (b) Sampling at sub-Nyquist rate, thus trading recovery accuracy for harvesting more energy.

By setting $f_s(\delta) = \frac{1}{T_{aq}+T_h(\delta)}$, *the solution to* (13) *is*

$$\zeta^o(\delta) = 1 - \frac{1}{\sigma_x^2}\sum_{k\in\mathcal{Z}}\int_{-\frac{f_s(\delta)}{2}}^{\frac{f_s(\delta)}{2}} \frac{|S_x(f-kf_s(\delta))|^2}{\sum_{k'\in\mathcal{Z}} S_x^H(f-k'f_s(\delta))}df. \tag{15a}$$

Similarly, by letting $T_s(\epsilon)$ *be the maximal sampling interval satisfying* $\zeta(T_s(\epsilon)) = \epsilon$ *in* (9), *the solution to* (14) *is*

$$E^o_{\text{ratio}}(\epsilon) = \frac{\frac{\eta}{R_h}(T_s(\epsilon) - T_{aq})\sigma_x^2}{a_2(n)K^2\sigma_x^2 + a_1(n)K\sigma_x}. \tag{15b}$$

Proof. The theorem follows as $\zeta(T_s)$ in (9) is monotonically decreasing in T_s, while E_{ratio} in (12) is a monotonically increasing with T_s. Thus, both (13) and (14) are obtained by identifying the minimal/maximal value of T_s for which the constraint holds with equality, proving the theorem. ■

In the following subsection we provide a few examples of energy-fidelity tradeoffs which arise from the above analysis.

3.4. Examples

The characterization of the energy-fidelity tradeoff in Theorem 2 identifies the achievable energy ratio for a given recovery accuracy and vice versa. It also reveals the achievable energy ratio when *e*Sampling a bandlimited signal of maximum frequency $f_m \geq 0$ with zero reconstruction error. In particular, combining Corollary 1 and Theorem 2 indicates that this energy ratio is given by

$$E^o_{\text{ratio}}(0) = \frac{\frac{\eta}{R_h}(\frac{1}{2f_m} - T_{aq})\sigma_x^2}{a_2(n)K^2\sigma_x^2 + a_1(n)K\sigma_x}. \tag{16}$$

An example of how Theorem 2 is computed for arbitrary sampling rates is given in the following:

Example 2 (*Flat PSD*). Consider again the bandlimited signal with flat PSD of Example 1. In this case, by (11), an NMSE of $\zeta(1/f_s) \leq \epsilon$ is guaranteed by using $f_s \geq 2f_m(1-\epsilon)$. Consequently, by Theorem 2 the energy ratio under fidelity constraint ϵ for such signals is given by

$$E^o_{\text{ratio}}(\epsilon) = \frac{\frac{\eta}{R_h}(\frac{1}{2f_m(1-\epsilon)} - T_{aq})\sigma_x^2}{a_2(n)K^2\sigma_x^2 + a_1(n)K\sigma_x}. \tag{17}$$

The resulting energy-fidelity tradeoff curve for different numbers of quantization bits is depicted in Fig. 5 under the following settings: We use $K^2 = 100$, guaranteeing a probability of over 99% that $|x(t)| \leq V_{\text{ref}}$, while the ADC circuit parameters are set to $f_m = 19.8$ MHz, $T_{aq} = 5$ ns, $C_u = 8.5$ fF, $C_c = 5$ fF, $C_s = 0.7$ fF, $R_h = 95.6\ \Omega$, $A_k = 1.8$, $V_e = 0.05$ V, $\alpha_\tau = 5$, $V_{\text{ref}} = 1$ V, $g = 0.4$, and $\eta = 11.6\%$. Finally, the signal power σ_x^2 is accordingly set to $\frac{V_{\text{ref}}^2}{K^2}$. These design parameters correspond to the *e*Sampling ADC circuit design presented in Section 4, and are in the typical ranges provided in previous works on ADC circuitry, e.g., [31,39,40]. The energy harvesting efficiency η is in line with similar values reported for energy harvesting circuits in [41–43].

As expected, the achievable energy ratio in Example 2 coincides with (16) when perfect recovery is required, i.e., $\epsilon = 0$. The energy ratio characterized in (17) is increased by reducing the sampling rate, which in turn increases the reconstruction error, ϵ, as illustrated in Fig. 4. The fundamental balance between these measures follows from the structure of *e*Sampling ADCs, in which increasing the hold time degrades the ability to recover the signal from its samples, while allowing to harvest more energy. This unique property of *e*Sampling enables ADCs to harvest significant fraction of energy that consume during acquisition, as observed in Fig. 5.

The example in Fig. 5 demonstrates that an n-bit *e*Sampling ADC acquiring a bandlimited signal can be fully self-powered when it samples below the Nyquist rate, and hence compromises on the reconstruction error. For instance, in Fig. 5 we observe that an 8-bit *e*Sampling ADC can harvest the same amount of energy it consumes for NMSE of $\zeta = 0.468$. Furthermore, $E_{\text{ratio}} = 0.47$ is achieved, while sampling at the Nyquist rate, and hence achieving (approximately) zero reconstruction error for signals with flat PSDs, as shown in Fig. 5. A similar observation holds for stationary signals with arbitrary PSDs that are bandlimited to f_m and have variance of σ_x^2. This follows since by (12), the energy ratio for a given sampling rate and signal variance does not depend on the shape of the PSD. We note that due to non-linearities arising

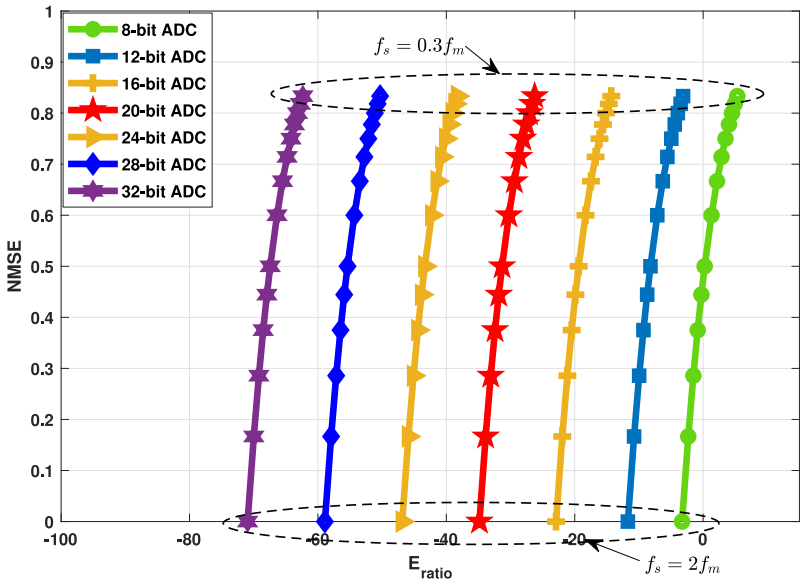

Fig. 5. NMSE (ζ) versus E_{ratio}, flat PSD.

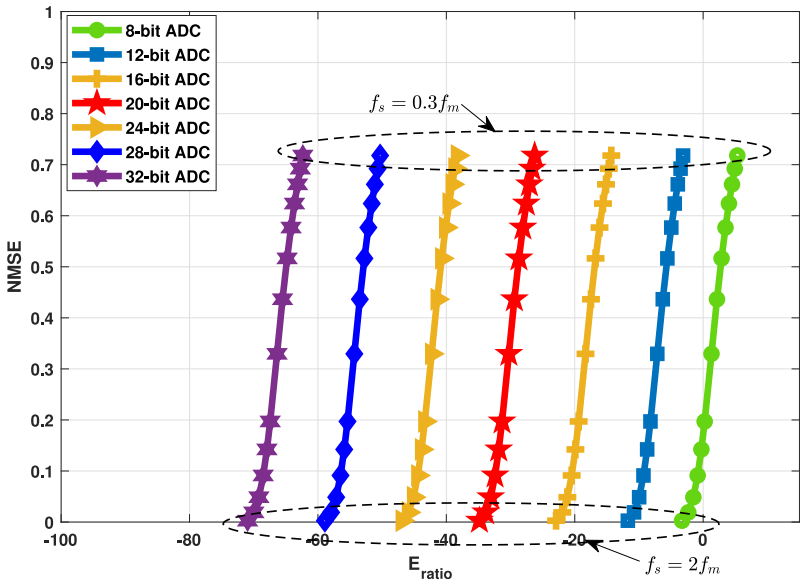

Fig. 6. NMSE (ζ) versus E_{ratio}, unimodal PSD.

practical setups, the achievable E_{ratio} is expected to be lower than that characterized here. In our practical experiment proof-of-concept detailed in Section 4.4, we experimentally achieve $E_{\text{ratio}} = 0.215$, i.e., 21.5% of the energy consumed in acquisition is harvested, when sampling at Nyquist rate.

It is emphasized that for a given sampling rate, *e*Sampling ADCs implement the same acquisition mapping as conventional S/H ADCs, and thus their ability to harvest energy using *e*Sampling ADCs does not come at the expense of conversion accuracy. However, *e*Sampling provides to the possibility to increase the amount of energy harvested by increasing the sampling interval, which in turn may degrade the recovery.

As mentioned above, the recovery NMSE depends not only on the sampling rate but also on the shape of the PSD $S_x(f)$ (9), however, the energy ratio for a fixed sampling rate is affected only by the overall input energy $\sigma_x^2 = \int S_x(f)df$ (12). This follows from the fundamental difference between the two objectives of *e*Sampling, i.e., acquisition and energy harvesting: The purpose of acquisition is to allow the complete signal, whose profile depends on the shape of its PSD, to be recovered from its digital representation. However, energy harvesting aims at extracting energy from the signal without having to maintain sufficiency or to avoid distorting the signal, and is invariant of the specific shape of its PSD. The dependency of the energy-fidelity tradeoff on the PSD profile is demonstrated in the following two examples which, unlike Example 2, consider non-purely-bandlimited signals:

Example 3 (*Unimodal PSD*)**.** Let $x(t)$ be a WSS signal with a PSD given by $S_x(f) = \alpha e^{-\frac{f^2}{2\sigma^2}}$, where $\alpha = \frac{\sigma_x^2}{\sqrt{2\pi\sigma^2}}$ such that $\int_{-\infty}^{\infty} S_x(f)df = \sigma_x^2$. The parameter σ^2 controls the PSD width, and is set to $\sigma = f_{\text{m}}/3$. The resulting energy-fidelity tradeoff computed via Theorem 2 under the ADC circuit parameters used in Example 2 is depicted in Fig. 6, along with an illustration of the PSD.

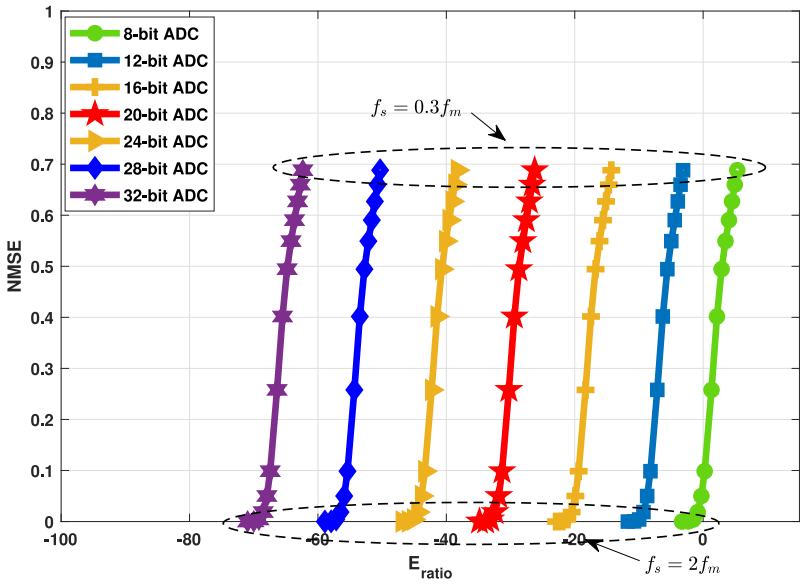

Fig. 7. NMSE (ζ) versus E_{ratio}, multimodal PSD.

Example 4 (*Multimodal PSD*). Let $x(t)$ be a WSS signal with a PSD $S_x(f) = \frac{\alpha}{2}(e^{-\frac{(f-f_m)^2}{2\sigma^2}} + e^{-\frac{(f+f_m)^2}{2\sigma^2}})$. Here, σ is set to $\sigma = f_m/6$. This PSD profile and the energy-fidelity tradeoff evaluated using Theorem 2 under the ADC circuit parameters used in Example 2 is depicted in Fig. 7.

The examples illustrated in Figs. 6 and 7 demonstrate that *e*Sampling ADCs applied to signals with such spectral profiles can operate at zero power with low normalized reconstruction error of 0.172 and 0.076, respectively, for $n = 8$ bits of quantization resolution. Observing Figs. 6–7 and comparing them to Fig. 5, we note that different PSD profiles lead to different energy-fidelity curves. This property is solely due to the dependence of the achievable NMSE on the PSD, which follows from Theorem 1, since both the amount of energy harvested from a stationary signal as well as that consumed in *e*Sampling do not depend on the spectral profile of the signal, but on the sampling rate and the variance σ_x^2. In particular, it is observed that *e*Sampling ADCs operating at n bits per sample are capable of saving power. However, this mode of operation comes at the cost of increased NMSE for higher values of n. In Section 4 we use a dedicated *e*Sampling ADC circuit proof-of-concept to demonstrate these results.

3.5. Discussion

Our characterization in the previous subsections focuses on the general family of stationary signals. When the signal obeys some structure, e.g., it is known to be sparse in the frequency domain, ideal recovery can be achieved at low sampling rates using generalized sampling methods [2], allowing to harvest energy without affecting the recovery NMSE. This indicates that the energy-fidelity tradeoff of *e*Sampling ADCs can be further improved by accounting for structured signals, as commonly encountered in communication [8] and radar [9] systems. We leave the analysis of *e*Sampling of structured signals for future work.

The fact that *e*Sampling gives rise to ADCs which can harvest energy, and hence makes it an attractive technology for low-power systems, such as internet of things devices, sensor networks, as well as wearable and implantable medical units. However, the applicability of the proposed *e*Sampling ADC is limited in some scenarios since its architecture is based on S/H ADCs. For example, S/H ADCs typically operate at sampling rates below 1 GHz, and are not suitable for operating at extremely high sampling rates, where flash ADCs are more commonly used. While we conjecture that the concept of *e*Sampling, namely, the integration of energy harvesting into signal acquisition, can also be combined with alternative ADC technologies other than S/H, we leave this for future study.

Our analysis focuses on WSS signals for analytical tractability; however, the proposed *e*Sampling ADC applies to a much broader family of acquired analog signals. For example the *e*Sampling ADC circuitry detailed in the following section is experimented when acquiring a sinusoidal signal, demonstrating its ability to accurately reconstruct the signal in a power saving manner. Furthermore, our proposed analysis is based on linear recovery, being a common reconstruction framework in sampling theory. In particular, the reconstruction of Nyquist rate sampled bandlimited signals, shift-invariant signals, and various other structures studied in the literature, is based on linear filtering [2]. However, the architecture of the *e*Sampling ADC is invariant to the reconstruction mechanism, and alternative recovery schemes would result in a different characterization of the energy-fidelity tradeoff.

4. *e*Sampling ADC circuit-level design

To demonstrate the hardware feasibility of *e*Sampling, we present a circuit-level design of such a device. We design an *e*Sampling ADC circuit based on the model in Fig. 2 using standard 65 nm CMOS technology, and study it using the Cadence Virtuoso platform. We design its three main sub-blocks: The two-way switch $\tilde{S}$; the quantizer logic; and the energy harvesting circuit. We elaborate on each of these sub-blocks, after which we present the experimental study.

4.1. Two-way switch

The two-way switch $\tilde{S}$ allows the input signal to be connected to the hold capacitor during acquisition phase and to the energy harvesting circuit during hold phase. In our design, $\tilde{S}$ is implemented[1] using two one-way switches, one for each operation phase, namely, when one switch is open, the other is closed. Each of the switches is realized using a different topology. The switch connecting the input signal to the energy harvesting circuit is implemented using a PMOS transistor,

[1] The term '*implement*' used here implies the design/simulation of the circuit in Cadence Virtuoso platform, in line with the similar usage of this terminology in [21–24,27].

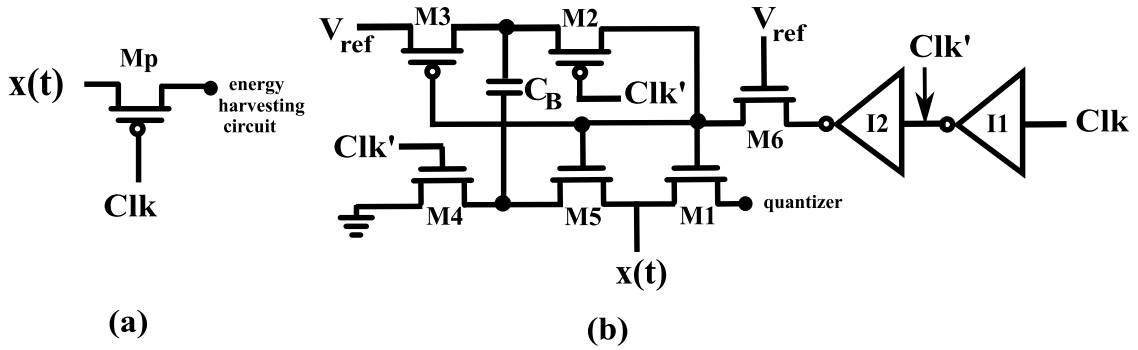

Fig. 8. Circuit diagram of (a) PMOS transistor switch, (b) NMOS bootstrapped switch.

as illustrated in Fig. 8(a). The PMOS transistor turns ON when the clock signal Clk is at logic '0', i.e., hold phase is active. When Clk is at logic '1', it turns OFF and isolates the input signal from the next block. In order to allow both switches of $\tilde{S}$ to utilize the same single clock pulse, the switch designed to connect the input signal with the quantizer is implemented using an NMOS transistor, which turns on when Clk is at '1'.

The on-resistance of a MOS transistor, which determines the value of R_{on} in (1), is sensitive to fluctuations in the input signal and may vary accordingly [25]. Such variations in R_{on} may introduce a non-linear distortion at the output of the ADC. To avoid such distortion, we use an NMOS bootstrap switch to connect the input signal to the quantizer, which ensures a constant R_{on}, as proposed in [44]. The design of the NMOS transistor based bootstrapped switch used in this work is illustrated in Fig. 8(b). To achieve nearly constant R_{on}, the gate of the transistor $M1$ in Fig. 8(b) is bootstrapped using two PMOS transistors $M2$ and $M3$, three NMOS transistors $M4$, $M5$ and $M6$, and one capacitor C_B, following [44]. Two CMOS inverters $I1$ and $I2$ are also employed in the structure to generate the required clock signals needed for proper operation of the switch.

The values of the on-resistance R_{on} and the hold capacitor C_h affect the setting of the acquisition time T_{aq} by (1). To maximize the amount of energy harvested, small values of T_{aq} are preferable, so that more time could be allocated to harvesting the input signal energy. Reducing R_{on} requires increasing the width of the transistors [25], which in turn increases the device capacitance, and thus reduces the operating speed of the ADC. In addition, wider devices may result in charge injection [45], which degrades the signal-to-noise-distortion ratio (SNDR) of the ADC, and hence the performance of the ADC. Alternatively, employing small values for C_h results in mismatch issues and sampling noise, which degrade the ADC conversion accuracy [46,47]. These drawbacks require the acquisition time T_{aq} to be large enough such that the ADC performance is not compromised, and is in fact the primary reason S/H ADCs are typically limited to operate with sampling rates below 1 GHz, as discussed in Section 3.5.

4.2. Quantizer

The dedicated *e*Sampling ADC circuit design is based on S/H SAR ADC architectures [26,31,48] as illustrated in Figs. 1–2. Such quantizers generally consist of a DAC, a voltage comparator and a SAR logic, which map the voltage of the hold capacitor (also known as the total capacitance of DAC array) into an n-bit value by successively refining the digital representation using a binary search algorithm. In our *e*Sampling ADC circuit we use a single-ended merge capacitor switching (MCS) based SAR ADC. For such devices, the total capacitance of the DAC array is $C_h = 2^{n-1}C_u$, where C_u is the unit capacitance of the DAC array, as illustrated in Fig. 9.

In particular, during acquisition phase the input signal $x(t)$ is connected to the top plate of the DAC capacitor array, while the bottom plate is connected to the common mode voltage, i.e., $V_{cm} = \frac{V_{ref}}{2}$. Once the acquisition phase is over, the voltage at the top plate of the DAC capacitor array is reduced by common mode voltage, and hence equals to $x(kT_s) - V_{ref}/2$. The top plate of the DAC capacitor array is connected to the positive terminal of the comparator, while the negative terminal of the comparator is grounded. The comparator then compares the voltage of its positive terminal with its negative terminal. If the voltage at the positive terminal is higher than the negative terminal, the comparator yields an output of logic '1', else logic '0'. The output of the comparator is passed to the SAR logic, which resolves the most significant bit (MSB). The decision on the MSB is fed back to the DAC and the bottom plate of the largest capacitor of DAC capacitor array is switched from V_{cm} to ground (if MSB = 1) or V_{ref} (if MSB = 0). This operation changes the voltage at the top plate of the DAC capacitor array, and a new decision is made by the comparator, which is sent to the SAR logic to resolve the second MSB and so on. The process continues for all n bits. The overall resistance of the switches is determined by the binary scale switch resistance, R_q, as illustrated in Fig. 9.

As discussed in Section 2.1, the energy consumption of S/H SAR ADCs is effectively dictated by its quantization sub-blocks. Therefore in the following, we detail the circuitry used for the quantizer along with its energy usage per sample.

The voltage comparator is implemented using a dynamic latch. The energy consumed per sample of a dynamic latch comparator is given by [31]

$$E_c = nC_cV_{ref}^2 + 2V_{ref}\gamma_n, \tag{18}$$

where $\gamma_n := V_eC_c\left(n\ln 1/A_k + \frac{n(n+1)}{2}\ln 2 + n\right)$, C_c is the capacitive load of the comparator, A_k is the gain during regenerative phase, and V_e is the ratio of the drain current of the device with its trans-conductance [39]. The SAR logic is realized using two arrays of shift registers that operate in serial-in-parallel-out and parallel-in-parallel-out modes [49]. Each register is implemented using a D flip-flop circuit, and the resulting energy consumption is given by [31]

$$E_{sl} = 16n^2\, gC_sV_{ref}^2, \tag{19}$$

where C_s is the input capacitance of the D flip-flop, and $g \in [0, 1]$ is the total activity parameter of the SAR logic. Finally, the DAC is based on a binary-weighted capacitive DAC, designed using the MCS scheme [26]. The energy consumption of the MCS DAC is given by [26]

$$E_{DAC} = \rho_nC_uV_{ref}^2, \tag{20}$$

where $\rho_n = \sum_{i=1}^{n-1} 2^{n-3-2i}(2^i - 1)$.

To summarize, the total energy consumption during hold phase of our dedicated *e*Sampling ADC circuit design, which dictates the overall energy consumed per sample, is given by

$$\begin{aligned} E_{hold} &= E_{DAC} + E_{sl} + E_c \\ &\overset{(a)}{=} V_{ref}^2\left(\rho_nC_u + nC_c + 16n^2C_sg\right) + 2V_{ref}\gamma_n, \end{aligned} \tag{21}$$

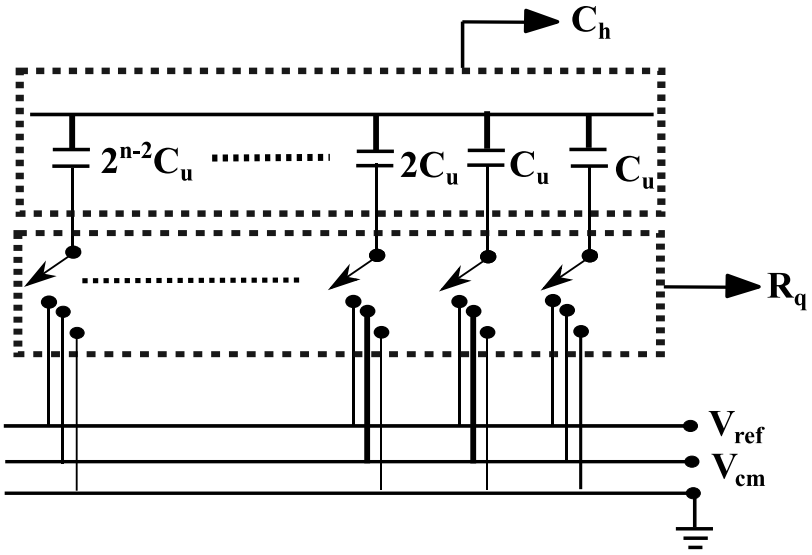

Fig. 9. DAC capacitor array schematic diagram.

where (a) follows from (18), (19), and (20). The energy term in (21) obeys the second-order polynomial model of (4), used in our analysis of *e*Sampling ADCs in Section 3.

4.3. Energy harvesting circuit

The proposed *e*Sampling ADC harvests the input signal energy during hold phase and stores this energy in a capacitor, C_{EH}. We do not focus in our description on the case where the harvested energy is utilized to power the ADC itself, as for that purpose additional regulation techniques are typically required. Nonetheless, one can use the harvested energy to drive other on-chip circuits, as we discuss in our experimental proof-of-concept in Section 4.4.

As detailed in Section 2.2, energy harvesting circuits typically consist of a capacitor, in which the harvested energy is stored, and a signal conditioning circuit, whose purpose is to facilitate the charging of the capacitor. In our design, we do not include a signal conditioning circuit and forward the input signal directly to C_{EH} during hold time. This simplified design is sufficient for our experimental purposes, where we use synthetic controlled input signals with strictly positive voltage values. However, in order to achieve efficient energy harvesting of a low voltage complex rapidly alternating signals, one should also include signal conditioning devices, such as a rectifier, voltage regulator, and DC-DC converter. We emphasize that our objective here is to demonstrate the proof-of-the-concept for the energy harvesting system using a simple capacitor model. However, in order to enhance the application scope of the proposed energy harvesting system to drive ICs (generate a stable output voltage), circuits, such as rectifiers can be deployed, which is considered for future extensions.

To quantify the maximum amount of energy that can be harvested in an analytically tractable manner, we consider the case where the input signal is approximately constant during the hold phase, i.e., $x(t) \approx x(T_s)$ for each $t \in [T_{\mathrm{aq}}, T_{\mathrm{s}}]$. The purpose of this approximation is to facilitate characterizing the amount of energy harvested in a tractable manner. In addition, we focus on the scenario in which the capacitor is empty at the beginning at the hold phase, namely, the voltage on the capacitor C_{EH}, denoted $V_{\mathrm{EH}}(0)$, satisfies $V_{\mathrm{EH}}(T_{\mathrm{aq}}) = 0$. In this setup, the capacitor voltage at the end of the hold phase, i.e., at time instance $t = T_{\mathrm{s}}$, is given by

$$V_{\mathrm{EH}}(T_{\mathrm{s}}) \approx x(T_s)\left(1 - e^{-\frac{T_{\mathrm{h}}}{R_{\mathrm{h}}C_{\mathrm{EH}}}}\right), \tag{22}$$

where, as defined in Section 3.1, R_{h} is the resistance of the energy harvesting circuit. This resistance is dictated here by the on-resistance of the PMOS transistor in the two-way switch. The amount of energy harvested in such a sampling interval is given by

$$\begin{aligned} E_{\mathrm{h}} &= \frac{1}{2}C_{\mathrm{EH}}V_{\mathrm{EH}}^2(T_{\mathrm{s}}) \\ &\overset{(a)}{\approx} \frac{1}{2}C_{\mathrm{EH}}\left(1 - e^{-\frac{T_{\mathrm{h}}}{R_{\mathrm{h}}C_{\mathrm{EH}}}}\right)^2 x^2(T_s) \\ &\overset{(b)}{\approx} \frac{1}{2T_{\mathrm{h}}}C_{\mathrm{EH}}\left(1 - e^{-\frac{T_{\mathrm{h}}}{R_{\mathrm{h}}C_{\mathrm{EH}}}}\right)^2 \int_{T_{\mathrm{aq}}}^{T_{\mathrm{s}}} |x(t)|^2 dt, \end{aligned} \tag{23}$$

where (a) follows from (22), and (b) stems from the fact that the input is approximately constant during the hold phase. Comparing (23) and (8) reveals that the efficiency of this simple energy harvesting circuit can be approximated as

$$\eta \approx \frac{R_{\mathrm{h}}C_{\mathrm{EH}}}{2T_{\mathrm{h}}}\left(1 - e^{-\frac{T_{\mathrm{h}}}{R_{\mathrm{h}}C_{\mathrm{EH}}}}\right)^2. \tag{24}$$

The expression for the energy harvesting efficiency in (24) can be used to provide guidelines for determining the capacitance C_{EH} used in the circuit. In particular, it can be shown that (24) is maximized when $C_{\mathrm{EH}} \approx 0.796\frac{T_{\mathrm{h}}}{R_{\mathrm{h}}}$. However, due to on-chip size limitation for practical setup, in our experimental proof-of-concept detailed in Section 4.4, we set $C_{\mathrm{EH}} = 0.239\frac{T_{\mathrm{h}}}{R_{\mathrm{h}}}$, resulting in the capacitor taking approximately 15 samples to charge up.

4.4. Simulation results

To validate the feasibility of *e*Sampling ADCs theoretically studied in Section 3, we experimentally evaluate an *e*Sampler circuit design. The purpose of this study is to serve as a proof-of-concept of *e*Sampling ADCs, using a relatively simple circuitry. To that aim, a schematic of the *e*Sampling ADC circuit has been created in Cadence Virtuoso platform based on the circuit-level design detailed in the previous subsections. The *e*Sampling ADC operates at a sampling frequency of 40 MHz with an $n = 8$ bit quantizer. For our experimental purpose, we use a sinusoidal signal, being a common benchmark for evaluating the accuracy of ADC circuits [50, Ch. 2]. The maximum frequency of the input signal is 19.8 MHz, thus the sampling rate satisfies the Nyquist condition. The amplitude of the signal varies from 0 to V_{ref}. Here, we use an energy harvesting capacitor of $C_{\mathrm{EH}} = 50$ pF. To demonstrate the application of *e*Sampling ADCs for the real-world systems, we used the

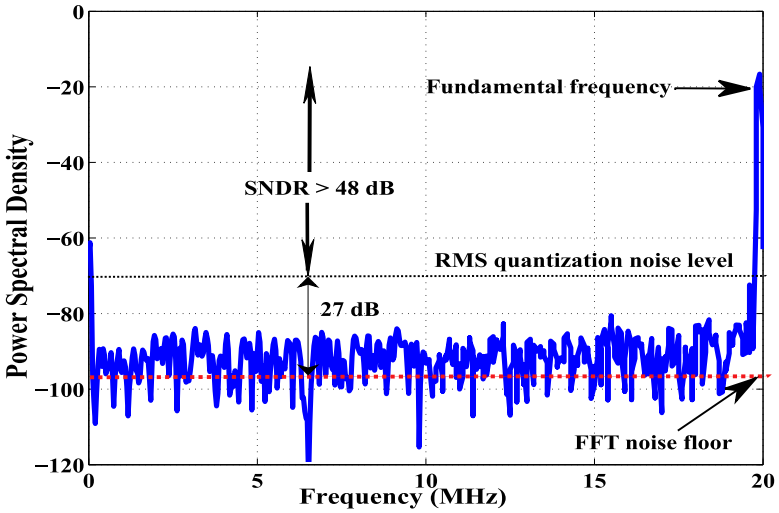

Fig. 10. FFT plot of reconstructed signal for 8-bit *e*Sampling ADC.

Table 1
Performance comparison of the proposed *e*Sampling ADC with other standard ADCs.

Specification	Proposed work	[51]	[52]
Tech.	65 nm	90 nm	40 nm
Supply (V)	1	1	0.9
Sampling rate (MS/s)	40	40	40
Resolution	8	8	12
ENOB	7.77	7.75	10.04
Power consumption (μW)	138	113	240

harvested energy in the capacitor to power a commonly used on-system circuitry: an operational amplifier (op-amp). The remaining parameters are the same those detailed in Example 2.

We first assert that the *e*Sampling ADC is indeed capable of accurately reconstructing the signal sampled at the Nyquist rate. To that aim, we depict the fast Fourier transform (FFT) of the reconstructed signal, computed using a 1024-point FFT, in Fig. 10. As expected, the FFT noise floor is determined by the SNDR due to quantization, computed by the 6 dB rule of thumb as approximately 48 dB, with the additional FFT processing gain of $10\log_{10}(1024/2) \approx 27$ dB [50, Ch. 2]. In particular, negligible level of noise coupling between the acquisition and energy harvesting circuits is observed, and the gap between the noise floor observed in Fig. 10 and the energy of the signal at its central frequency of 19.8 MHz, is roughly 75.52 dB. This settles with the theoretical performance of Nyquist-rate ADCs, and indicates that the designed *e*Sampling ADC accurately reconstructs the observed analog signal.

In Table 1, the performance measures of *e*Sampling ADC are mentioned, and its comparison with the standard S/H ADCs is also drawn. This comparison clearly shows that performance metric of the proposed *e*Sampling ADC is in-line with standard ADC performance. Therefore, it is established that the proposed *e*Sampling harvesting system can be integrated with any S/H ADC without comprising its standard performance.

Next, we focus on the energy harvesting and energy consumption of the designed *e*Sampling circuit. The average amount of energy harvested per sample is 0.74 pJ, evaluated using (23). Furthermore, the average energy consumption of our designed circuit is 3.44 pJ. This is computed by evaluating the current drawn from its reference source V_{ref}, denoted $I_{\text{ref}}(t)$, and thus the energy consumed at each time instance can be obtained by

$$E_{\text{cons}}(t) = V_{\text{ref}} \int_0^t I_{\text{ref}}(\tau) d\tau. \tag{25}$$

For this setting, the ratio of the harvested energy to that consumes is evaluated as $E_{\text{ratio}} = 21.5\%$. This demonstrates that in practical designs, one can harvest a reasonable (over 20%) amount of the consumed energy using the eSampling circuit, as a proof-of-the concept, without impacting the reconstruction accuracy and with minimal additional circuit worth of a single capacitor. To our understanding, this is the first work demonstrating that energy can be harvested from the waveform thrown away between two successive samples during sampling of an analog signal. Additionally, if the existing energy harvesting systems are deployed alongside this proposed system set-up, it can lead to greater improvements in the future generation devices that may become self-sustaining in power requirements.

In order to identify how many sampling rounds are required for the capacitor to charge up, we plot in Fig. 11 the voltage on the energy harvesting capacitor over time. Observing Fig. 11, we note that for the given input signal, the capacitor reaches a steady level of $V_{\text{EH}} = 660$ mV after 0.372 μs, which corresponds to 15 samples at 40 MHz. The voltage level produced by the energy harvesting circuit includes ripples and noise, as observed in Fig. 11. To demonstrate that this harvested energy is suitable for driving on-chip circuits, we use V_{EH} as a power supply to power up an op-amp. We implemented a two-stage low voltage op-amp [53] and performed its schematic level analysis in Cadence Virtuoso. Since the ripple in V_{EH} is varying from 672 mV to 603 mV, the circuit performance is validated by accomplishing via AC analysis at 672 mV and 603 mV, and the results are depicted in Figs. 12 and 13, respectively. It is observed in Figs. 12–13 that the op-amp performs optimally even in the presence of the introduced ripples, obtaining more than 60 dB gain and more than 45° phase margin [54, Ch. 6].

To further assert the usefulness of *e*Sampling, we conducted an experiment by disconnecting the energy harvesting capacitor C_{EH} from the eSampling ADC after 0.372 μs (as shown in Fig. 15) when C_{EH} is fully charged. The detached harvesting capacitor is then used to power the op-amp, while its recharging from *e*Sampling ADC remained discontinued. A V_{EH} value of atleast 561 mV is required for maintaining a phase margin of 45°. As shown in Fig. 14, it is found that the op-amp can be driven by the detached harvesting capacitor for 7.29 μs, which is much greater than the time required to charge harvesting capacitor. Therefore, the proposed system of one harvesting capacitor can be extended to power more than one on-system circuit by employing time based switching circuit at the harvesting branch of the *e*Sampling system.

Finally Fig. 15 describes the variations in voltage level across the energy harvesting capacitor when an additional on-system circuitry (op-amp in our experiment) is continuously derived by the harvested voltage V_{EH}. Through Figs. 11 and 15, we can also observe that

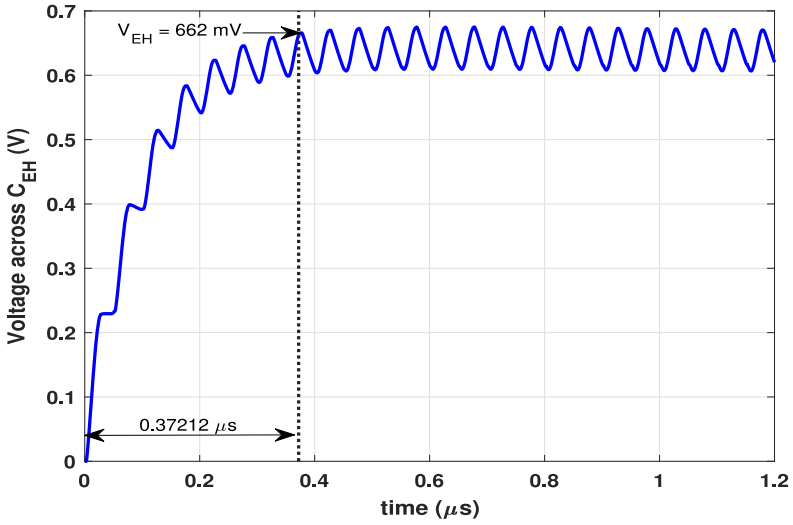

Fig. 11. Voltage obtained across C_{EH} for 8-bit, when no other circuitry is connected to harvesting branch *e*Sampling ADC.

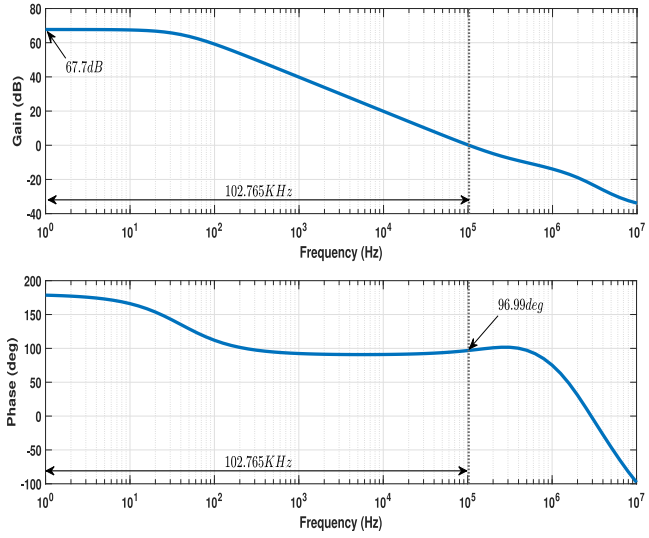

Fig. 12. AC analysis of op-amp at maximum voltage transient point $V_{EH} = 672$ mV.

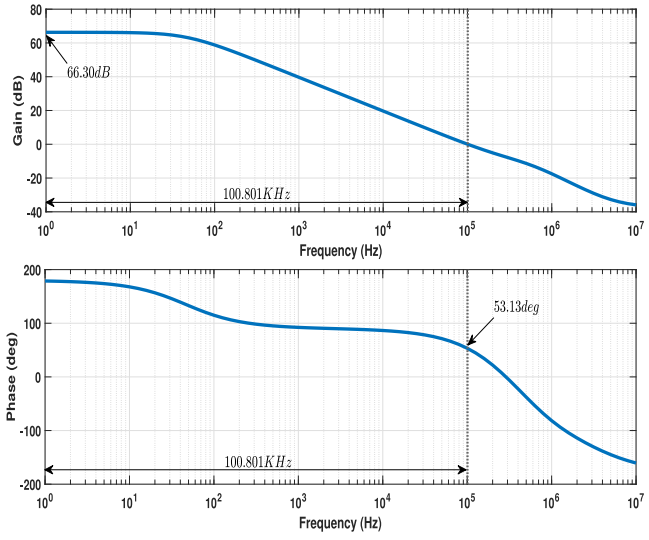

Fig. 13. AC analysis of op-amp at minimum voltage transient point $V_{EH} = 603$ mV.

connecting the harvesting branch with an op-amp produces a meagre impact on the charging time and peak voltage of the harvesting capacitor. Further, a voltage regulator [55,56] circuit can be developed to mitigate the ripples produced in the harvested voltage (V_{EH}). It can be taken as an interesting future direction to develop an *e*Sampling system with optimized energy harvester circuit. Such an *e*Sampling system will be helpful to provide regulated power supply for driving on-chip circuits. We therefore conclude that the current simplified design can be used to power a few more on-chip circuits without compromising on the reconstruction accuracy. In particular, using more advanced harvesting architecture can increase the efficiency η, allowing to achieve improved energy-fidelity tradeoffs compared to those observed here. Nonetheless, despite its relatively simple architecture, the *e*Sampling ADC circuit design is clearly shown to be able to achieve accurate reconstruction while harvesting an amount of energy that is comparable to its consumed energy.

This is to note that the performance of energy harvested will not be degraded under noise interference or temperature variations, although the performance of ADC may be impacted. This is a practical issue related to the ADCs in general, although when the ADC are designed with standard (matured) semiconductor technologies, they typically show a reliable and robust dynamic performance. For example, one may refer to the following SAR ADC data sheets from Texas Instruments [57] and Analog devices [58], where an almost stable and robust dynamic performance of the ADCs is observed. In fact, eSampling ADC does not interfere with the working of the traditional ADC and hence, would not impact its performance under various conditions or alter its performance under temperature or noise scenarios. The objective of this study is to show the proof-of-concept of energy harvesting during analog sampling. In any practical application, care has to be taken on the functional aspects of the designed circuits to ensure robust performance. This is to further clarify that since the idea is to harvest energy between successive samples while sampling an analog signal, the proposed system would be able to harvest energy from the noisy or wideband signals as well within the operating frequency range of the accompanying system (e.g. ADC and sampling switch in this case). However, for harvesting energy from RF signals or very high frequency signals, there are different strategies in the literature [19].

5. Conclusion

In this paper, we proposed the *e*Sampling ADC architecture, which modifies the traditional conversion process of a S/H ADC to harvest energy from the discarded portion of the input signal. We analyzed

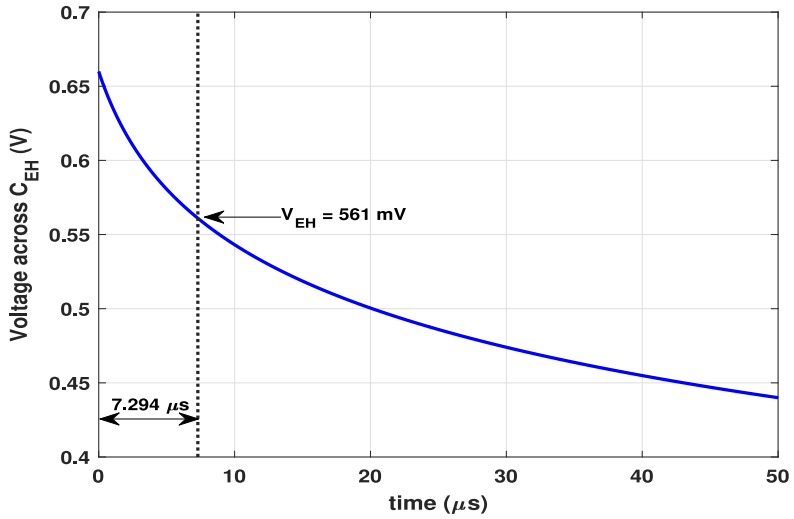

Fig. 14. Energy Depletion of the charged harvesting capacitor from 660 mV to lowest required V_{DD} of 561 mV for powering the op-amp.

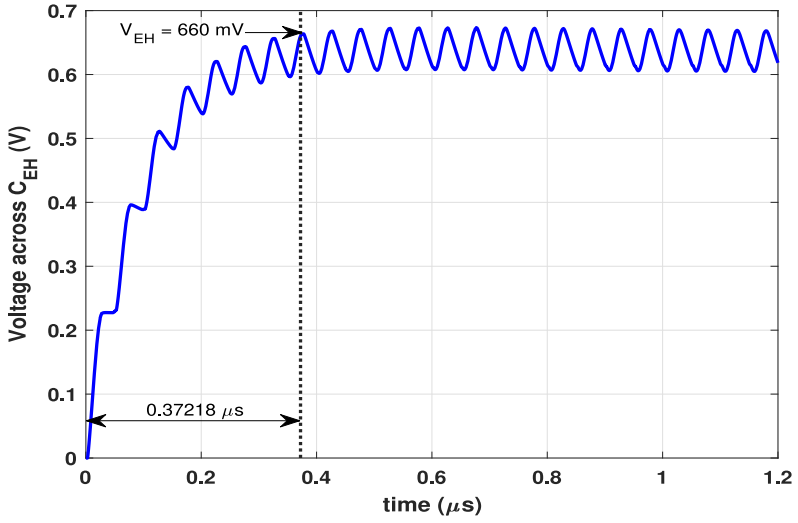

Fig. 15. Voltage obtained across C_{EH} for 8-bit *e*Sampling ADC, when op-amp is connected to harvesting branch.

the amount of energy which can be harvested from stationary signals and characterized the underlying fundamental tradeoff between harvested energy and reconstruction fidelity. Our theoretic characterization shows that an *e*Sampling ADC can harvest significant fraction of consumed power during acquisition, when sampling both bandlimited signals and non-bandlimited at a sampling rate allowing recovery with negligible error. Then, we presented a circuit-level design of an 8-bit *e*Sampling ADC on CMOS 65 nm technology to demonstrate the feasibility of proposed system. The experimental results shows that the proposed ADC system can harvest 21.5% of its consumed energy, while recovering the analog signal perfectly. Finally, we implemented a circuit-level design of a practical op-amp device and successfully powered it using the harvested energy of the implemented *e*Sampling system. This experiment establishes the significance of proposed system by entirely powering an op-amp device, which is a frequently used on-system circuit of ADC systems.

CRediT authorship contribution statement

Neha Jain: Writing – review & editing, Writing – original draft, Visualization, Validation, Software, Methodology, Investigation, Formal analysis, Conceptualization. **Nir Shlezinger:** Writing – review & editing, Writing – original draft, Visualization, Validation, Supervision, Software, Methodology, Investigation, Formal analysis. **Bhawna Tiwari:** Writing – review & editing, Visualization, Validation, Investigation, Formal analysis. **Harsh Verma:** Writing – review & editing, Visualization, Investigation, Formal analysis. **Yonina C. Eldar:** Writing – review & editing, Validation, Supervision, Resources, Project administration, Methodology, Formal analysis. **Pydi Ganga Bahubalindruni:** Writing – review & editing, Validation, Supervision, Methodology, Formal analysis. **Vivek Ashok Bohara:** Writing – review & editing, Writing – original draft, Supervision, Resources, Project administration, Methodology, Investigation, Funding acquisition, Conceptualization. **Anubha Gupta:** Writing – review & editing, Writing – original draft, Supervision, Resources, Project administration, Methodology, Funding acquisition, Formal analysis, Conceptualization.

Ethics statement

During the preparation of this work, the author(s) did not use any AI tool.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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