

RF Chain Reduction for MIMO Systems: A Hardware Prototype

Tierui Gong^{ID}, *Student Member, IEEE*, Nir Shlezinger^{ID}, *Member, IEEE*,
Shahar Stein Ioushua^{ID}, *Student Member, IEEE*, Moshe Namer,
Zhijia Yang^{ID}, and Yonina C. Eldar^{ID}, *Fellow, IEEE*

Abstract—Radio frequency (RF) chain circuits play a major role in digital receiver architectures, allowing passband communication signals to be processed in baseband. When operating at high frequencies, these circuits tend to be costly. This increased cost imposes a major limitation on future multiple-input-multiple-output (MIMO) communication technologies. A common approach to mitigate the increased cost is to utilize hybrid architectures, in which the received signal is combined in analog into a lower dimension, thus reducing the number of RF chains. In this article we study the design and hardware implementation of hybrid architectures via minimizing channel estimation error. We first derive the optimal solution for complex-gain combiners and propose an alternating optimization algorithm for phase-shifter combiners. We then present a hardware prototype implementing analog combining for RF chain reduction. The prototype consists of a specially designed configurable combining board as well as a dedicated experimental setup. Our hardware prototype allows us evaluating the effect of analog combining in MIMO systems using actual communication signals. The experimental study, which focuses on channel estimation accuracy in MIMO channels, demonstrates that using the proposed prototype, the achievable channel estimation performance is within a small gap in a statistical sense from that obtained using a costly receiver in which each antenna is connected to a dedicated RF chain.

Index Terms—Channel estimation, hybrid receivers, multiple-input-multiple-output (MIMO) communications.

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Tierui Gong is with the Key Laboratory of Networked Control Systems, State Key Laboratory of Robotics, Shenyang Institute of Automation, Chinese Academy of Sciences, Shenyang 110016, China, and the Institutes for Robotics and Intelligent Manufacturing, Chinese Academy of Sciences, Shenyang 110169, China, and also with the University of Chinese Academy of Sciences, Beijing 100049, China (e-mail: gongtierui@sia.cn).

Nir Shlezinger and Yonina C. Eldar are with the Faculty of Mathematics and Computer Science, Weizmann Institute of Science, Rehovot 76100, Israel (e-mail: nirshlezinger1@gmail.com; yonina@weizmann.ac.il).

Shahar Stein Ioushua is with the School of Electrical Engineering, Tel Aviv University, Tel Aviv 6997801, Israel (e-mail: shunbunstein@gmail.com).

Moshe Namer is with the Faculty of Electrical Engineering, Technion, Haifa 32000, Israel (e-mail: namer@ee.technion.ac.il).

Zhijia Yang is with the Key Laboratory of Networked Control Systems, State Key Laboratory of Robotics, Shenyang Institute of Automation, Chinese Academy of Sciences, Shenyang 110016, China, and also with the Institutes for Robotics and Intelligent Manufacturing, Chinese Academy of Sciences, Shenyang 110169, China (e-mail: yang@sia.ac.cn).

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I. INTRODUCTION

NEXT-generation wireless systems are required to meet a growing throughput demand [1]. Two key technologies offer the potential of providing dramatic increase in spectral efficiency. The first scheme equips the cellular base stations (BS) with a large number of antennas, realizing a massive multiple-input-multiple-output (MIMO) system [2]–[4]. The second method explores the millimeter wave frequency band, overcoming the congestion of the conventional spectrum [5]. A major drawback of utilizing these technologies stems from the fact that radio frequency (RF) chain circuits, which allow the passband communication signals to be processed in baseband (BB) and are, thus, an essential component in digital receiver architectures, lead to increased cost and power consumption when operating at high carrier frequencies. This increased cost becomes a major practical bottleneck when implementing MIMO antenna arrays operating at millimeter wave bands in which each antenna is connected to an RF chain.

One of the common approaches to mitigate this increased cost is to utilize fewer RF chains [6]–[8], namely, implementing RF chain reduction. This reduction is carried out by introducing additional analog hardware, which most commonly consists of controllable phase shifters and adders [6], typically designed to optimize the achievable rate [7] or the channel estimation accuracy [8]. In such systems, the analog signal observed at the antenna array is combined into a lower dimension digital signal using dedicated hardware [9]. When utilizing such hybrid architectures, the number of RF chains, and, hence, the number of inputs processed in the digital domain is smaller than the number of antennas. Receiver designs implementing RF chain reduction using analog combining have been the focus of extensive research in recent years [9]–[23]. These previous works include the design of different analog combining structures [9], [13]–[15], [20], [21], hybrid architectures with low-resolution analog-to-digital conversion [10], [11], [16]–[19], [22], and the integration of dynamic analog combining as part of the physical antenna technology [12]. The theoretical maturity of the concept of MIMO communications with RF chain reduction suggests the need to demonstrate and evaluate the implementation of such systems in hardware, which is the focus of this article.

We present a prototype of a configurable analog combining hardware board. Our analog combiner hardware can realize different RF chain reduction strategies, including complex gain combiners [22], [23], phase shifter networks [9], [13],

and antenna selection techniques [18]. The board is designed to experimentally evaluate MIMO communications with RF chain reduction applied to actual up-converted passband signals. Similarly to [24] and [25], we design a dedicated analog combiner hardware for experimental purposes. While [25] used RF integrated circuits, focusing on millimeter wave bands, our prototype targets the sub-6 GHz frequency range, as in [24]. The main advantage of our prototype over [24] is in the improved phase resolution, which stems from the usage of dedicated vector multipliers, allowing to more accurately set the phase of the complex coefficients and, thus, to better test analytically derived analog combiners. While our prototype supports a smaller number of antennas compared to [24], we propose a method for using it to experiment in scenarios with larger number of antennas using a virtual channel extension.

Our main design criteria is the channel estimation accuracy, using an analog combining configuration algorithm, which extends and improves upon the method suggested in [13]. The proposed algorithm uses alternating optimization to obtain a suitable analog combining configuration under structure constraints, such as the requirement to utilize unit gain coefficients arising in phase shifter networks. Our method achieved closer feasible approximations of the optimal unconstrained combiner compared to the algorithm of [13] by introducing an additional degree of freedom, which is exploited to improve the approximation under structure constraints. While we focus on the task of channel estimation, the proposed prototype can be used to implement analog combiners designed according to alternative objectives, e.g., maximize the achievable rate as in [16], or signal recovery, as suggested in [13].

The proposed hardware prototype, which combines our specially designed analog combiner board with a dedicated experimental hardware setup, demonstrates the feasibility of hybrid architectures in wireless networks. In particular, we show that, using a phase shifter network configured with our analog combiner board and the proposed design algorithm, one can achieve channel estimation accuracy, which is within a small gap from that achievable using a MIMO receiver with a complex controllable gain combiner.

The main contributions of the article are summarized below.

- 1) We study the design of analog combiners to maximize channel estimation accuracy. To that aim, we first derive the optimal solution for complex-gain hybrid combiner in the noisy setting, extending the derivation in [14, Section IV], which considered noiseless settings. We show that the combiner is not unique, and specializes to that of [14] in the high signal-to-noise ratio (SNR) regime.
- 2) Then, we propose an algorithm for designing constrained hybrid beamformers, focusing on the common phase-shifter network architecture [9]. Our method is based on alternating optimization, i.e., joint optimization by iteratively optimizing over one quantity while keeping the other variables fixed extending the previously proposed method of [13]. Our algorithm builds upon the nonuniqueness of the complex-gain solution to find the one, which can be best approximated using a feasible combiner setting.
- 3) Finally, we present a dedicated hardware prototype operating in the sub-6 GHz band, with configurable complex

gains of extremely high phase resolution, allowing reliable comparison of different hybrid architectures using passband signals. The prototype is used for evaluating our method, demonstrating its ability to approach the performance of variable gain combiners using constrained phase shifters.

The rest of this article is organized as follows: In Section II, we formulate the model for wireless communication with RF chain reduction and present the channel estimation problem. Section III details the algorithm implemented for configuring the analog combiner, and Section IV presents a detailed description of the prototype and its components. Experimental results are given in Section V, and Section VI provides concluding remarks.

Throughout the article, we use boldface lowercase letters to denote vectors, e.g., \mathbf{x} , and the i th element of \mathbf{x} is written as $(\mathbf{x})_i$. Boldface uppercase letters are used for matrices, e.g., \mathbf{M} , whose (i, k) th entry is $(\mathbf{M})_{i,k}$ and i th column is $(\mathbf{M})_{:,i}$. We use $\text{vec}(\cdot)$ to denote the vectorization operator, \mathbf{I}_n is the $n \times n$ identity matrix, \otimes is the Kronecker product, $\|\cdot\|$ is the l_2 norm, $\|\cdot\|_F$ is the Frobenius norm, $\text{tr}(\cdot)$ is the trace operator, while $(\cdot)^T$ and $(\cdot)^*$ denote the transpose and complex transpose, respectively. The proper-complex Gaussian distribution is denoted as \mathcal{CN} , and \mathbb{C} is the set of complex numbers. The expectation of a random variable x is represented by the operator $\mathbb{E}\{x\}$.

II. SYSTEM MODEL

Our hardware prototype implements RF chain reduction for MIMO receivers. In particular, we design the hybrid architecture to facilitate channel estimation in multi-antenna cellular BS. To formulate the setup and the design objectives, we first detail the problem formulation in Section II-A, after which we present the considered model for the unknown channel in Section II-B.

A. Problem Formulation

Consider a single-cell network in which a BS is equipped with N_{bs} antennas and serves K single-antenna user terminals (UTs). We focus on the uplink, namely, the transmission from the UT to the BS. The BS utilizes an analog combiner, and, thus, observes the channel output after it has been linearly combined and acquired using $N_{rf} \leq N_{bs}$ RF chains. The analog combiner network is denoted via the matrix $\mathbf{W} \in \mathcal{W}$, where $\mathcal{W} \subseteq \mathbb{C}^{N_{rf} \times N_{bs}}$ represents the feasible set of analog combiners. This set is determined by the specific hardware of the analog combiner, and can represent, e.g., complex gains and phase shifter networks [9], [13].

Let $\mathbf{H} \in \mathbb{C}^{N_{bs} \times K}$ denote the wireless channel matrix and $\mathbf{S} \in \mathbb{C}^{\tau \times K}$ be the transmitted symbols of all the UT in the cell over τ time instances. We can express the received BB signal via

$$\mathbf{Y} = \mathbf{W}\mathbf{H}\mathbf{S}^T + \mathbf{W}\mathbf{N} \quad (1)$$

where $\mathbf{N} \in \mathbb{C}^{N_{bs} \times \tau}$ represents the additive white Gaussian noise (AWGN) corrupting the channel output, modeled as having i.i.d. zero-mean proper-complex Gaussian entries with variance $p_n > 0$. The resulting model is illustrated in Fig. 1.

Our hardware prototype implements the analog combining matrix \mathbf{W} . In particular, we consider two different feasible sets for the analog combining weights \mathcal{W} .

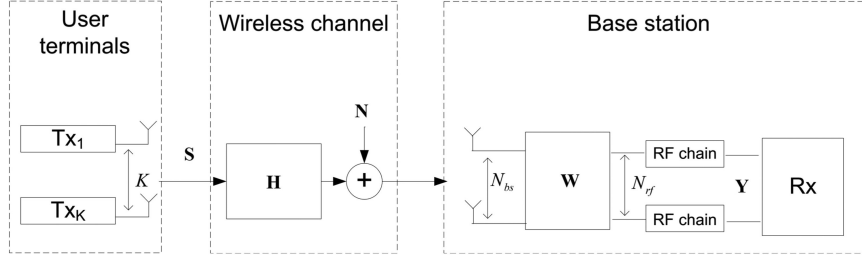


Fig. 1. BB communication system diagram.

- 1) **Complex-Gain Analog Combiner (CGAC):** Such analog combiners can realize any form of analog combining, namely, $\mathcal{W} = \mathbb{C}^{N_{rf} \times N_{bs}}$. This architecture is implemented using a hardware network with controllable gains and phase shifters.
- 2) **Phase-Shifter-Only Analog Combiner (PSOAC):** Here, the elements of the combiner matrix have a fixed unit magnitude. Such analog combiners are implemented using adjustable phase shifters, and, thus, tend to be less costly and simpler to implement compared to CGAC.

Since we focus on facilitating channel estimation, we design the analog combining hardware to minimize the mean-squared error (MSE) in recovering the channel matrix \mathbf{H} from the observed channel output \mathbf{Y} . We assume that \mathbf{S} represents an *a-priori* known orthogonal pilot sequence, i.e., that channel estimation is carried out in a pilot-aided fashion, where $\mathbf{S}\mathbf{S}^* = \mathbf{I}_\tau$ and $\tau \geq K$. The design objective can, thus, be formulated as

$$\mathbf{W}^o = \arg \min_{\mathbf{W} \in \mathcal{W}} \mathbb{E} \left\{ \|\mathbf{H} - \mathbb{E}\{\mathbf{H}|\mathbf{Y}\}\|_F^2 \right\}. \quad (2)$$

We emphasize that the proposed approach can also be extended to multiple cells, in which the channel output is corrupted by an additional interference term, as well as to signal recovery scenarios. In signal recovery, the observed output \mathbf{Y} in (1) is used to recover the transmitted symbols \mathbf{S} , assuming that knowledge of the channel matrix \mathbf{H} (or a reliable estimate of it) is available.

B. Channel Model

We consider MMSE estimation of the unknown channel matrix \mathbf{H} from the channel output \mathbf{Y} . We model the distribution of the channel matrix using the common Kronecker model [26]–[28]. Accordingly, the matrix \mathbf{H} can be written as

$$\mathbf{H} = \mathbf{Q}^{\frac{1}{2}} \bar{\mathbf{H}} \mathbf{P}^{\frac{1}{2}} \quad (3)$$

where $\mathbf{Q} \in \mathbb{C}^{N_{bs} \times N_{bs}}$ and $\mathbf{P} \in \mathbb{C}^{K \times K}$ are the deterministic nonsingular receive side and transmit side correlation matrices, respectively; and $\bar{\mathbf{H}} \in \mathbb{C}^{N_{bs} \times K}$ models Rayleigh fading, i.e., its entries are i.i.d. zero-mean unit variance proper-complex Gaussian random variables (RVs). We, henceforth, assume that the transmit side correlation matrix is a scalar multiple of the identity matrix, i.e., $\mathbf{P} = \alpha \mathbf{I}_K$ for some $\alpha > 0$, representing the scenario in which the UT are distributed in the cell in an i.i.d. manner. The correlation matrices \mathbf{Q} and \mathbf{P} are assumed to be known to the BS, and can be utilized for recovering the unknown channel \mathbf{H} , as discussed in the following section.

Our motivation for focusing on the Kronecker model (3) with $\mathbf{P} = \alpha \mathbf{I}_K$ stems from the fact that this facilitates deriving the optimal unconstrained CGAC, i.e., the solution to (2) when $\mathcal{W} = \mathbb{C}^{N_{rf} \times N_{bs}}$. Nonetheless, our algorithm for designing PSOAC, detailed in Section III, is not restricted to a specific model and only requires an unconstrained CGAC to approximate. Furthermore, our hardware prototype detailed in Section IV is model independent, and can support any analog combiner configuration.

III. ANALOG COMBINER DESIGN ALGORITHM

We now detail the proposed algorithm for designing the analog combining matrix \mathbf{W} based on the objective (2). Our method improves upon the minimal gap iterative quantization (MaGiQ) algorithm suggested in [13]: we begin by reformulating the MSE objective as a matrix trace expression, and then show how this objective can be utilized to design the analog combiner.

A. MSE Objective

In order to specialize the MSE objective (2) to our channel model detailed in Section II-B, we write the channel input–output relationship (1) in vector form. In particular, it holds from (1) that $\mathbf{y} \triangleq \text{vec}(\mathbf{Y})$ can be written as

$$\mathbf{y} = (\mathbf{S} \otimes \mathbf{W}) \mathbf{h} + (\mathbf{I}_\tau \otimes \mathbf{W}) \mathbf{n} \quad (4)$$

where $\mathbf{h} \triangleq \text{vec}(\mathbf{H}) \sim \mathcal{CN}(\mathbf{0}, \mathbf{P} \otimes \mathbf{Q})$ is the unknown channel in vector form and $\mathbf{n} = \text{vec}(\mathbf{N}) \sim \mathcal{CN}(\mathbf{0}, p_n \mathbf{I}_{N_{bs} \cdot \tau})$ is the additive noise. Since \mathbf{h} and \mathbf{n} are mutually independent, it follows from (4) that \mathbf{y} and \mathbf{h} are jointly Gaussian. Hence, the MMSE estimator is given by the linear MMSE estimator [29, Ch. 8], which can be written as

$$\hat{\mathbf{h}} \triangleq \mathbb{E}\{\mathbf{h}|\mathbf{y}\} = (\mathbf{P}\mathbf{S}^* \otimes \mathbf{Q}\mathbf{W}^*) \times [(\mathbf{S}\mathbf{P}\mathbf{S}^* \otimes \mathbf{W}\mathbf{Q}\mathbf{W}^*) + p_n (\mathbf{I}_\tau \otimes \mathbf{W}\mathbf{W}^*)]^{-1} \mathbf{y}. \quad (5)$$

Accordingly, the MSE $\epsilon \triangleq \mathbb{E}\{\|\mathbf{h} - \hat{\mathbf{h}}\|^2\}$ is given by [29, Ch. 8.4]

$$\epsilon = \text{tr}(\mathbf{P} \otimes \mathbf{Q}) - \text{tr}((\mathbf{P}\mathbf{S}^* \otimes \mathbf{Q}\mathbf{W}^*) [(\mathbf{S}\mathbf{P}\mathbf{S}^* \otimes \mathbf{W}\mathbf{Q}\mathbf{W}^*) + p_n (\mathbf{I}_\tau \otimes \mathbf{W}\mathbf{W}^*)]^{-1} (\mathbf{S}\mathbf{P}^* \otimes \mathbf{W}\mathbf{Q}^*)). \quad (6)$$

The MSE (6) is determined by the pilot symbols \mathbf{S} , the second-order statistical moments of the channel, represented by the correlation matrices \mathbf{Q} , \mathbf{P} , and the analog combiner \mathbf{W} . We next assume that \mathbf{S} , \mathbf{P} and \mathbf{Q} are known and seek the optimal combiner \mathbf{W} that minimizes the MSE of (6).

B. Analog Combiner Design

Minimization of (6) is equivalent to maximization of the second trace term of (6), i.e.,

$$\mathbf{W}^o = \arg \max_{\mathbf{W} \in \mathcal{W}} f(\mathbf{W}) \quad (7)$$

where

$$f(\mathbf{W}) = \text{tr}((\mathbf{P}\mathbf{S}^* \otimes \mathbf{Q}\mathbf{W}^*)[(\mathbf{S}\mathbf{P}\mathbf{S}^* \otimes \mathbf{W}\mathbf{Q}\mathbf{W}^*) + p_n(\mathbf{I}_T \otimes \mathbf{W}\mathbf{W}^*)]^{-1}(\mathbf{S}\mathbf{P}^* \otimes \mathbf{W}\mathbf{Q}^*)). \quad (8)$$

Let \mathcal{U} and \mathcal{D} be the sets of unitary $N_{rf} \times N_{rf}$ matrices and diagonal $N_{rf} \times N_{rf}$ matrices with positive diagonal entries. The analog combiner matrix \mathbf{W}^o for unconstrained analog combiners, i.e., $\mathcal{W} = \mathbb{C}^{N_{rf} \times N_{bs}}$, is given in the following theorem.

Theorem 1: Let \mathbf{U}^o be an $N_{bs} \times N_{rf}$ matrix whose columns are the N_{rf} eigenvectors of $\bar{\mathbf{Q}}$ corresponding to its N_{rf} largest eigenvalues, where

$$\bar{\mathbf{Q}} \triangleq (\alpha\mathbf{Q} + p_n\mathbf{I}_{N_{bs}})^{-\frac{1}{2}}(\alpha\mathbf{Q})^2(\alpha\mathbf{Q} + p_n\mathbf{I}_{N_{bs}})^{-\frac{1}{2}}. \quad (9)$$

Then, for any $\mathbf{V} \in \mathcal{U}$ and $\mathbf{D} \in \mathcal{D}$, the optimization problem (7) is solved by setting

$$\mathbf{W}^o = \mathbf{V}\mathbf{D}(\mathbf{U}^o)^*. \quad (10)$$

Proof: The proof is detailed in Appendix A. ■

We note that in the high SNR regime, i.e., when $p_n \approx 0$, \mathbf{U} in Theorem 1 becomes the first N_{rf} eigenvectors of $\alpha\mathbf{Q}$, coinciding with the derivation in [14, Section IV], which assumed a noiseless setup.

The analog combiner in (10) is achievable for any \mathbf{V} and \mathbf{D} using the CGAC architecture, in which each element of the analog combining matrix can be any complex value. For the PSOAC case, the entries of the combiner matrix are restricted to have unit amplitude, a condition, which may not be satisfied for a matrix of the form (10). Following [13], we propose to exploit the nonuniqueness of \mathbf{W}^o to facilitate its approximation using a feasible PSOAC matrix. In particular, we recover the selection of the nonunique \mathbf{V} and \mathbf{D} for which the resulting \mathbf{W}^o can be closely approximated using a feasible \mathbf{W} , namely, our design objective is

$$\mathbf{W}^{po} = \arg \min_{\mathbf{W} \in \mathcal{W}, \mathbf{V} \in \mathcal{U}, \mathbf{D} \in \mathcal{D}} \|\mathbf{W} - \mathbf{V}\mathbf{D}(\mathbf{U}^o)^*\|_F^2. \quad (11)$$

In [13, Section V], only the nonuniqueness in the unitary \mathbf{V} is exploited, and the diagonal \mathbf{D} is assumed to be the identity matrix $\mathbf{I}_{N_{rf}}$. Consequently, our proposed design criterion generalizes that of MaGiQ [13], and is capable of recovering PSOAC matrices which better approximate the unconstrained MSE minimizing analog combiner compared to MaGiQ [13].

We tackle the optimization problem (11) in an alternating fashion. Our design method is based on the following lemma.

Lemma 1: For any fixed $\mathbf{V} \in \mathcal{U}$ and $\mathbf{D} \in \mathcal{D}$, if \mathcal{W} represents PSOAC matrices then

$$\tilde{\mathbf{W}} = \arg \min_{\mathbf{W} \in \mathcal{W}} \|\mathbf{W} - \mathbf{V}\mathbf{D}\mathbf{U}^*\|_F^2 = \mathcal{P}(\mathbf{V}\mathbf{D}\mathbf{U}^*) \quad (12a)$$

where $[\mathcal{P}(\mathbf{U})]_{ij} \triangleq e^{j2\pi\angle[\mathbf{U}]_{ij}}$ is the projection operator. Furthermore, for any $\mathbf{W} \in \mathcal{W}$ and $\mathbf{D} \in \mathcal{D}$, by letting \mathbf{L} and \mathbf{R}

Algorithm 1: Iterative Alternating Algorithm for PSOAC Matrices.

- 1: **Input:** Receive side correlation matrix \mathbf{Q} .
 - 2: **Output:** $\mathbf{W}^{po} \in \mathcal{W}$ (with unit magnitude entries).
 - 3: **Initialization:** $i := 0$, $\mathbf{V}_i := \mathbf{I}_{N_{rf}}$ and $\mathbf{D}_i := \mathbf{I}_{N_{rf}}$.
 - 4: Compute \mathbf{U} as the first N_{rf} eigenvectors of $\bar{\mathbf{Q}}$ in (9).
 - 5: **while** termination criterion is inactive **do**
 - 6: Obtain \mathbf{W}_{i+1} via (12a) with $\mathbf{V} = \mathbf{V}_i$ and $\mathbf{D} = \mathbf{D}_i$.
 - 7: Obtain \mathbf{V}_{i+1} via (12b) with $\mathbf{W} = \mathbf{W}_{i+1}$ and $\mathbf{D} = \mathbf{D}_i$.
 - 8: Obtain \mathbf{D}_{i+1} via (12c) with $\mathbf{W} = \mathbf{W}_{i+1}$ and $\mathbf{V} = \mathbf{V}_{i+1}$.
 - 9: $i := i + 1$.
 - 10: **return** $\mathbf{W}^{po} = \mathbf{W}_i$.
-

be the left and right singular vectors matrices of $\mathbf{W}\mathbf{U}\mathbf{D}$, respectively, it holds that

$$\tilde{\mathbf{V}} = \arg \min_{\mathbf{V} \in \mathcal{U}} \|\mathbf{W} - \mathbf{V}\mathbf{D}\mathbf{U}^*\|_F^2 = \mathbf{L}\mathbf{R}^*. \quad (12b)$$

Finally, letting $\eta > 0$ be some lower bound on the diagonal entries of the matrices in \mathcal{D} , guaranteeing that these values are strictly positive, it holds that for any $\mathbf{W} \in \mathcal{W}$ and $\mathbf{V} \in \mathcal{U}$, the diagonal entries of $\tilde{\mathbf{D}} = \arg \min_{\mathbf{D} \in \mathcal{D}} \|\mathbf{W} - \mathbf{V}\mathbf{D}\mathbf{U}^*\|_F^2$ are given by

$$(\tilde{\mathbf{D}})_{l,l} = \max \left(\frac{\text{Re}((\mathbf{W}^*\mathbf{V})_{:,l}^*(\mathbf{U})_{:,l})}{\|(\mathbf{U})_{:,l}\|^2}, \eta \right) \quad (12c)$$

for all $j = 1, \dots, N_{bs}$.

Proof: The lemma directly follows from [12, Lemma 2]. ■

Lemma 1 implies that the optimization problem (11) can be solved using alternating optimization. In particular, we propose to update each of the three matrices \mathbf{W} , \mathbf{V} , and \mathbf{D} in turn, while fixing the remaining two matrices, and to repeat this process iteratively. Since our objective in (11) is the minimization of the convex Frobenius norm, it follows from [30, Th. 2] that the convergence of such an alternating approach is guaranteed. The proposed iterative alternating optimization method is summarized in Algorithm 1. For a given \mathbf{U}^o , MaGiQ [13] can be considered as a special case of the proposed algorithm with \mathbf{D} fixed to the identity matrix, i.e., without step 8. This additional degree of freedom allows our algorithm to obtain close feasible approximations of the unconstrained optimal analog combiner \mathbf{W}^o , at the cost of the additional computation of the N_{rf} diagonal entries of \mathbf{D} in each iteration via (12c).

The fact that our algorithm obtains a better approximation of \mathbf{W}^o compared to MaGiQ also translates to the improved channel estimation accuracy, as demonstrated in the following example. Consider a multiuser MIMO system in which a BS equipped with $N_{bs} = 80$ antennas and $N_{rf} = 20$ RF chains serves $K = 40$ UT. The receive side correlation matrix \mathbf{Q} follows the Jakes' model with antenna spacing of 0.2 carrier wavelength [31], and the transmit side correlation \mathbf{P} is set to \mathbf{I}_K . In Fig. 2 we evaluate the normalized MSE, defined as $\frac{\epsilon}{\mathbb{E}\{\|\mathbf{h}\|^2\}}$, versus SNR, given

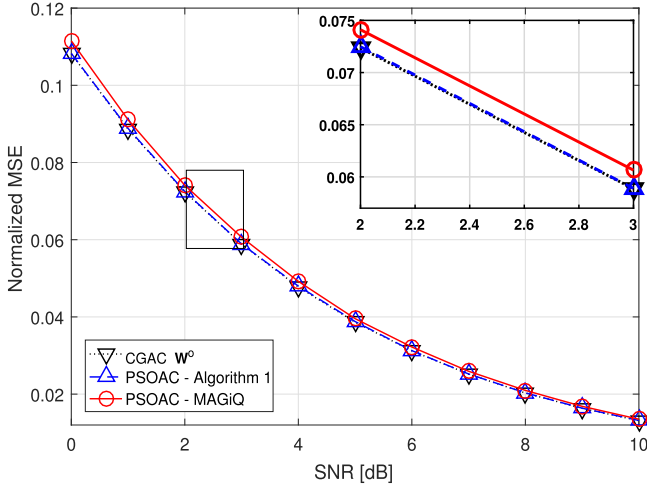


Fig. 2. Normalized MSE versus SNR, $N_{bs} = 80$, $N_{rf} = 20$.

by $SNR = p_n^{-1}$. The normalized MSEs are computed using the unconstrained CGAC W^o as well as PSOAC designed using MaGiQ and the proposed algorithm, respectively. Observing Fig. 2, we note that the PSOAC designed using the proposed algorithm achieves effectively the same performance as the CGAC W^o , which requires controllable gains, while the normalized MSE achieved using MaGiQ is within a small gap from W^o . This small gap in normalized MSE can lead to substantial gaps in MSE, particularly when the Frobenius norm of the channel, $\mathbb{E}\{\|\mathbf{h}\|^2\}$, is large, as common in massive MIMO systems. This numerical study demonstrates the superiority of the proposed algorithm over previous PSOAC design methods. Consequently, our hardware prototype and its experimental system use Algorithm 1 when realizing PSOAC.

In our prototype, we implement both CGAC, designed via (10) by setting $\mathbf{V} = \mathbf{D} = \mathbf{I}_{N_{rf}}$, and PSOAC, configured using Algorithm 1. The architecture of the prototype, which allows it to implement the aforementioned hybrid design in a dynamic manner, is discussed in the following section.

IV. SYSTEM ARCHITECTURE

In this section, we elaborate on the system architecture of the hardware prototype, which realizes the RF chain reduction scheme detailed in the previous section. To that aim, we first present the high-level system architecture in Section IV-A, after which we discuss the concrete structure of each of the hardware components in Section IV-B.

A. High-Level Design

1) *Experimental Environment*: Our hardware prototype implements a configurable analog combiner, which is evaluated using a dedicated experimental setup at microwave frequencies. This setup consists of a MATLAB-based host application and an FPGA board. The former simulates the BB channel output and processes the signal captured after analog combining. The latter acts as an interface between the digital signals generated and

processed by the host application, and the analog signals, which are utilized by the analog combiner hardware. In particular, the input and output signals of the analog combiner hardware are generated as follows.

- 1) *Analog Combiner Input*: The digital BB channel outputs simulated by the host application are transferred by an Ethernet cable from the host application to the FPGA board in real time. The FPGA board generates the BB input signal, which is up-converted on the combiner board using a carrier waveform generated by a VSG25 A vector signal generator. The resulting analog passband signal represents the multivariate channel output observed at the BS antenna array.
- 2) *Analog Combiner Output*: The analog combined passband signal, representing the signal fed to the RF chains at the BS, is down-converted with the same carrier waveform as for the up-conversion on the combiner board, followed by an analog-to-digital conversion implemented on the FPGA. These digital outputs are transferred from the FPGA board to the host application where they are utilized for estimating the underlying channel.

The host application is also capable of adjusting the weights of the analog combining hardware via the FPGA board. The experimental procedure is illustrated in the flowchart at the top of Fig. 3.

2) *Analog Combiner Implementation*: Several different architectures for analog combiners can be found in the literature [9], [13]: The most common is arguably a controllable network of fully connected phase shifters, i.e., the PSOAC. Alternative architectures include fully connected complex gain networks, such as the CGAC; fully connected phase shifters and switches network, and flexible partially connected phase shifters network with subarrays. We refer the readers to [9, Section II] for a detailed account of these analog combining architectures. In order to incorporate a large family of architectures, our analog combiner hardware consists of a controllable network of gains and phase shifters. The outputs of the adjustable gains and phase shifters are, then, summed by a combiner and fed to an RF chain. In particular, our hardware system consists of four input ports and two output ports, namely, it can be utilized in a BS with four antennas and two RF chains. This setup can also be used for experimenting with analog combiners with larger number of antennas and RF chains using a virtual channel extension.

By using the flexible and controllable network of gains and phase shifters, we implement the proposed designs for both CGACs as well as PSOACs. The baseline is to use the hardware board, which models a MIMO BS with four antenna inputs and two RF chains. While this combiner implements a hybrid MIMO receiver with $N_{bs} = 4$ and $N_{rf} = 2$, it can also be used, along with the experimental setup detailed in the sequel, to evaluate in hardware hybrid MIMO BS with eight antenna inputs and four RF chains as well as 16 antenna inputs and eight RF chains. The ability to use the board and the experimental setup to evaluate hybrid receivers with larger number of antennas and RF chains is obtained using a virtual channel extension. This

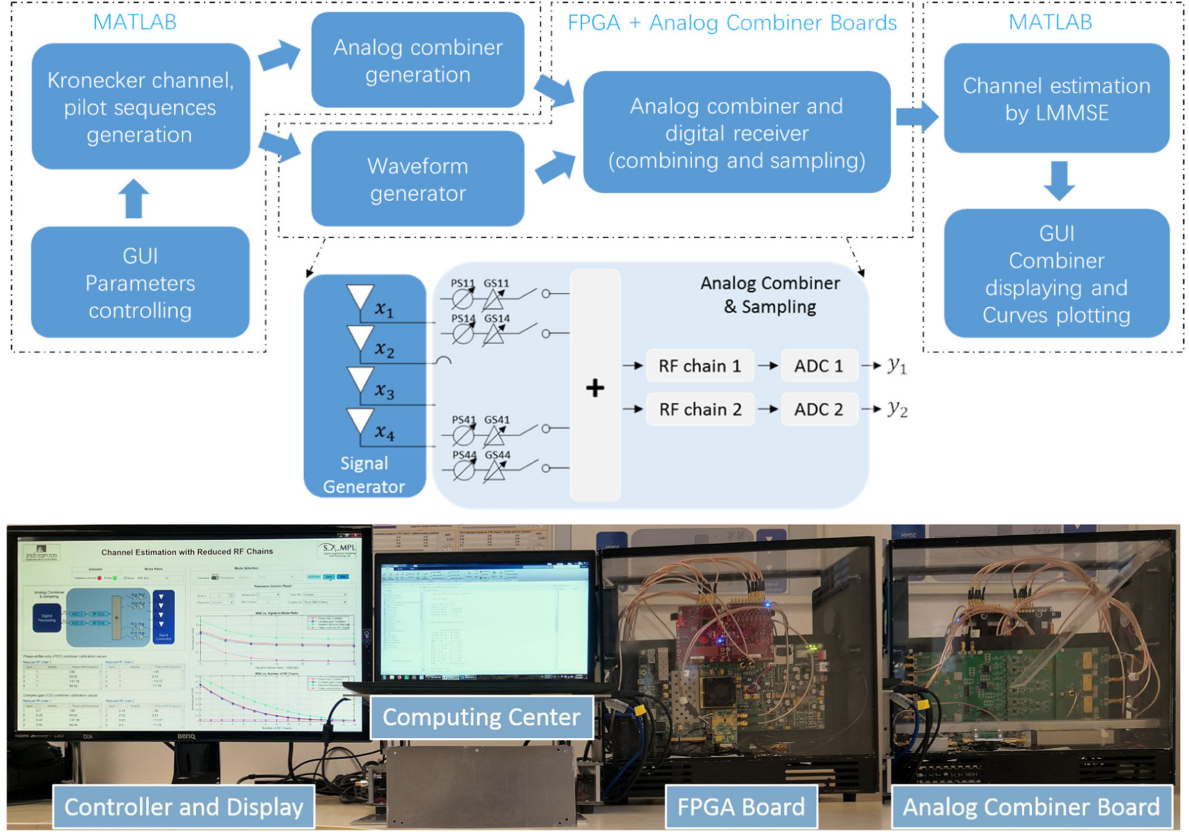


Fig. 3. (Top) Overview of the information flow in the experimental setup. (Bottom) Overview of the prototype and its subsystems.

virtual channel approach is based on a sequential utilization of the basic hardware to obtain an overall combined result.

To present the virtual channel extension, we note that the two outputs of the analog combiner are obtained as a linear combination of four antenna inputs with different weights, which are determined by some basic combining matrix \mathbf{W}_b . Defining $\mathbf{X}_b \triangleq \mathbf{H}\mathbf{S}^T + \mathbf{N}$, we denote the channel output with this basic combination as

$$\mathbf{Y}_b = \mathbf{W}_b \mathbf{X}_b. \quad (13)$$

In order to simulate more antenna inputs and RF chains, we utilize multiple time instances to form a single analog combining input–output pair. For example, in order to realize eight antenna inputs and four RF chain, we use two different 4×1 channel output vectors, denoted \mathbf{X}_b^1 and \mathbf{X}_b^2 , and four 4×2 analog combining matrices $\mathbf{W}_b^{11}, \mathbf{W}_b^{21}, \mathbf{W}_b^{12}, \mathbf{W}_b^{22}$. Now, following (13), we can obtain a configurable 8×4 analog combiner via the assignment

$$\begin{bmatrix} \mathbf{Y}_b^1 \\ \mathbf{Y}_b^2 \end{bmatrix} = \begin{bmatrix} \mathbf{W}_b^{11} & \mathbf{W}_b^{12} \\ \mathbf{W}_b^{21} & \mathbf{W}_b^{22} \end{bmatrix} \begin{bmatrix} \mathbf{X}_b^1 \\ \mathbf{X}_b^2 \end{bmatrix}. \quad (14)$$

It follows from (14) that we need to sequentially utilize the basic hardware four times to complete the divided four blocks of the analog combiner matrix. Following the same approach as the realization of eight antenna inputs and four RF chains, a setup with 16 antenna inputs and eight RF chains can be obtained by utilizing 16 different 4×2 basic combiners to complete the divided 16 blocks of the analog combiner matrix. Clearly, analog

combiners with different analog combining ratios, namely, in which the number of antennas is not twice the number of RF chains, can be realized following the same guidelines by using only the required number of input and output ports.

B. Prototype Physical Entities

The overall prototype system is depicted at the bottom of Fig. 3. The prototype consists of the following components: a controller and display, providing the graphical user interface (GUI), a computing center running the MATLAB-based host application, an FPGA board, and the analog combiner hardware. In the following, we elaborate on each of these blocks.

1) *Controller and Display*: The GUI allows us to configure and evaluate the experimental setup in a user-friendly environment. In particular, our GUI provides the ability to change the main parameters of the experiment and to numerically compare the normalized MSE obtained in two display modes: with respect to SNR or number of RF chains. The main controllable parameters include the number of UT, training symbols, receive antennas, and the rank of the receive side correlation matrix. Details of the supported parameter combinations are summarized in Table I.

Once the experimental setup is configured and a test is launched, the GUI presents in real time the selected values used to configure the analog combining hardware for both PSOAC as well as CGAC. Furthermore, the GUI presents updated normalized MSE curves during the test and after it is concluded,

TABLE I
CONTROLLABLE PARAMETERS SUPPORTED BY GUI

Working mode	Simulation		Hardware
Curve display mode	NMSE vs. SNR	NMSE vs. N_{rf}	NMSE vs. SNR
Number of UTs	$K = 1, \dots, 10$		
Number of training symbols	$\tau = 1 \times K, \tau = 2 \times K, \tau = 3 \times K$		
Number of receiving antennas in the BS	$N_{bs} = 4, N_{bs} = 8, N_{bs} = 16$		
Number of RF chains in the BS	$\frac{N_{bs}}{2}$	$2, \dots, N_{bs}$	$\frac{N_{bs}}{2}$
Rank of receive side correlation matrix	Regular case: $N_{rf} < rank \leq N_{bs}$, Best case: $rank = N_{rf}$		

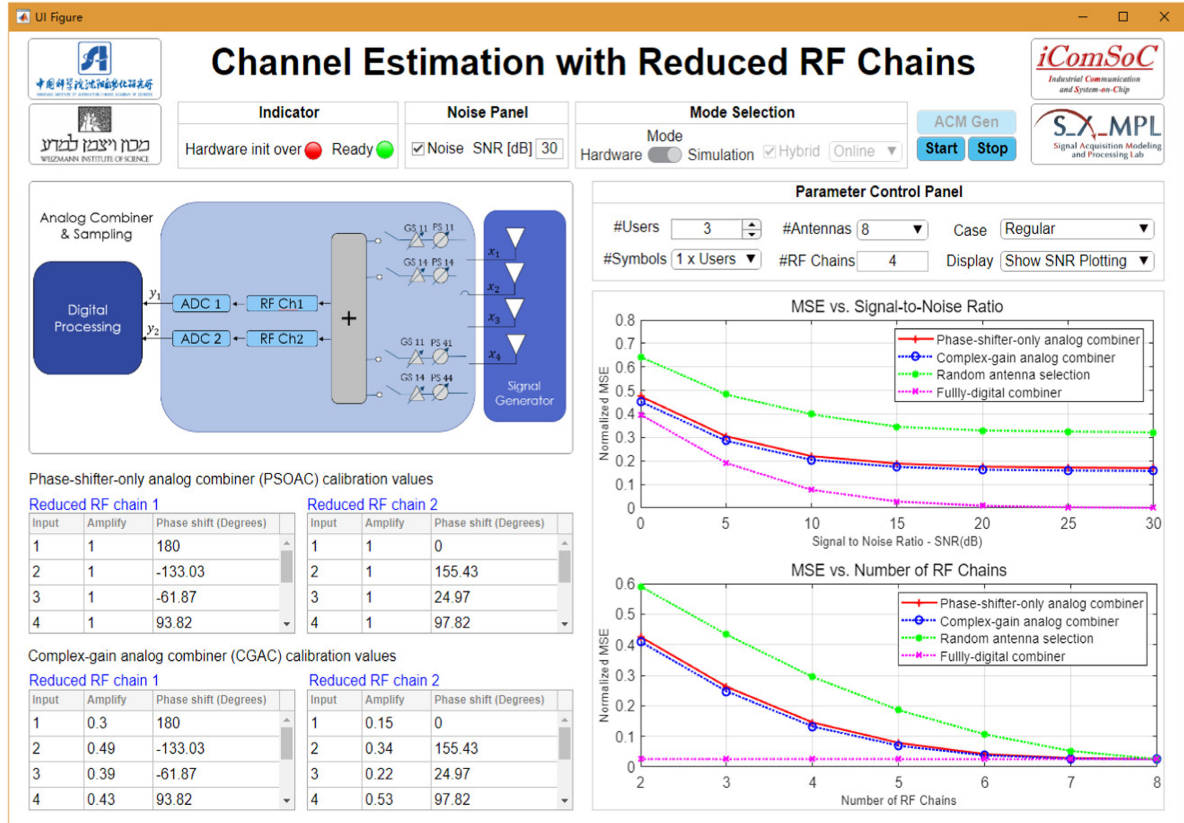


Fig. 4. Overview of the GUI.

comparing the performance of the utilized PSOAC and CGAC to analog combiners in which the RF chains are directly connected to randomly selected antennas, as well as to a fully digital setup. The fully digital setup, representing the performance achievable without analog combining when each antenna feeds a dedicated RF chain, constitutes a fundamental lower bound on the channel estimation MSE with RF chain reduction. An overview of the GUI is depicted in Fig. 4.

2) *Computing Center*: The computing center is a 64-bit laptop with four CPU cores and 16 GB RAM running the MATLAB-based host application. The application is controlled by the GUI, and implements the following functionalities.

- 1) The host application computes the analog combiner weights using the algorithm detailed in Section III, and adjusts the analog combiner hardware before each simulation test.
- 2) The application generates the digital BB signals, i.e., the pilot sequences, as well as the wireless channel outputs,

which are fed to the FPGA to generate the analog combiner input.

- 3) On the receive side, the application processes the BB channel outputs and produces the MMSE channel estimate via (5).

The communication between the computing center and the hardware board is carried out over an Ethernet cable. Through the cable, the generated digital BB channel outputs and analog combiner matrix are transmitted to the build-in memory of the FPGA board, and the BB RF chain outputs are acquired.

3) *FPGA Board*: The FPGA board consists of an off-the-shelf Xilinx VC707 evaluation board. The evaluation board utilizes a 4DSP FMC204 16-bit digital-to-analog converter (DAC) mezzanine card for BB waveform generation, as well as an eight-channel 4DSP FMC168 16-bit digitizer card for sampling of the combined analog signal.

In the BB analog signal generation process, the waveforms are stored as digital BB I/Q pairs on the build-in memory.

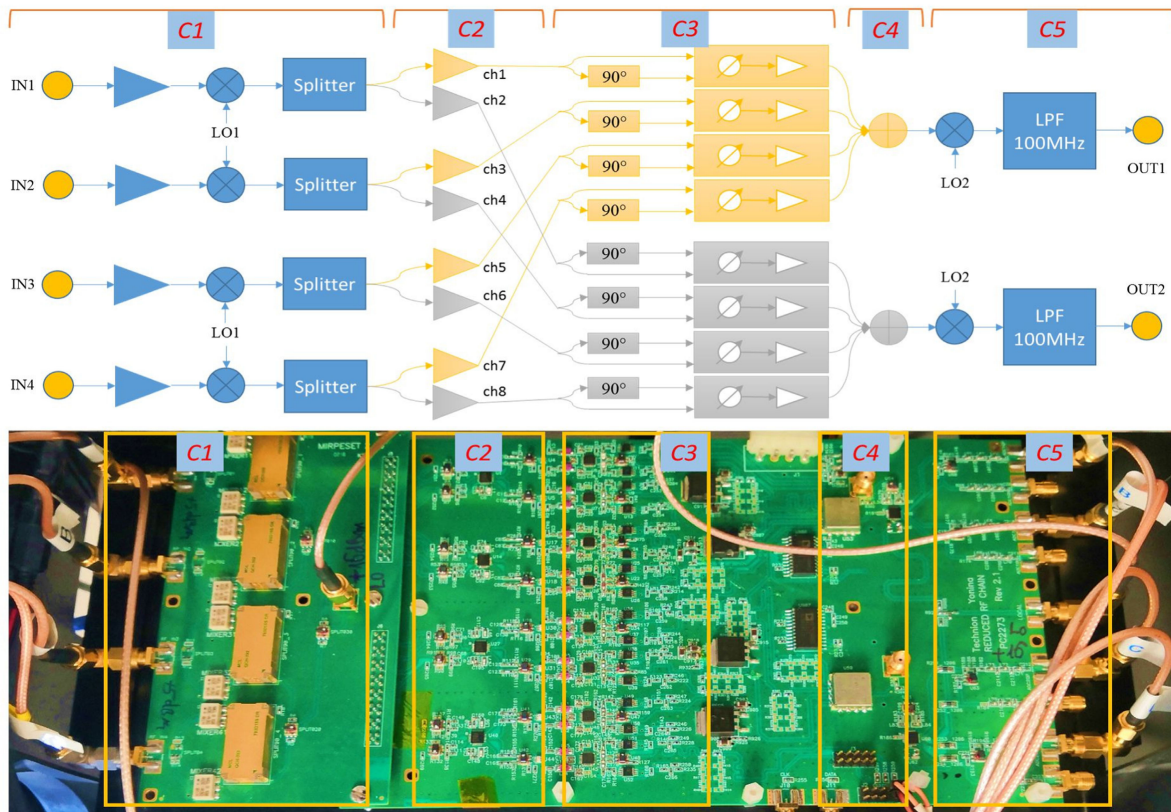


Fig. 5. Overview of the analog combiner board. Top: block diagram. Bottom: circuit board.

Then, the FPGA device reads out the prestored waveforms from the memory and employs an eight Gbps Serializer/Deserializer (SerDes) device to transfer it to the 16-bit DAC mezzanine card. The DAC card, then, interpolates and converts the stored waveforms to analog BB signals at a sample rate of 250 Msps. The analog BB signals are transmitted to the analog combiner board through coaxial cables where they are up-converted to passband and linearly combined.

The analog combiner outputs, which are down-converted to BB on the combiner board, are digitized using four out of eight channels of the 16-bit digitizer card with a 250 MHz sampling rate. Each I/Q pair occupies two channels of the digitizer card. The 1.2 Gb/s SerDes transfers the sampled data to the FPGA who, then, writes the data to a digital first-in first-out (FIFO) buffer for reading by the computing center.

The FPGA also produces selection and control commands for configuring of analog combiner. Once the host application produces an analog combiner configuration, the weights matrix is provided to the FPGA board via the FIFO buffer. These weights are, then, transferred to the analog combiner hardware using a serial peripheral interface protocol, which is used to control the dedicated analog combiner board.

4) *Analog Combiner Board*: The analog combiner board is a self-designed dedicated hardware, which realizes a controllable analog combiner network, and can serve as any of the common combiner architectures, e.g., phase shifter networks, switching networks [13], and discrete Fourier transform (DFT) beamforming [21]. The designed analog combiner supports two

different types of input signals: one is passband signals in the frequency band up to 4.5 GHz and another is BB signals each with a 125 MHz maximum bandwidth. In our experimental setup, we use BB signals as our inputs, where up-conversion and down-conversion are carried out on the analog combiner board. The board consists of five different blocks, implementing the main different functionalities, namely:

- 1) up-conversion of incoming signal and signal splitting;
- 2) passband signal input and amplification;
- 3) weights (phases and gains) application and configuration;
- 4) summing up of the incoming signals;
- 5) down-conversion and low-pass filtering of combined signals.

The individual blocks of the analog combiner board are marked in Fig. 5, which depicts the block diagram of the hardware as well as the circuit board.

In block 1, each of the four inputs is a complex BB signal transmitted from the FPGA, feeding an amplifier followed by a mixer. The BB signals whose maximal range of frequency is 125 MHz are up-converted to RF signals at a frequency of 1 GHz. The RF signals represent the passband signals observed by the BS antennas and each power level of the RF signals are tuned to 0 dBm and split into two same signals. In order to support passband inputs, one must only replace block 1 with the corresponding passband signals observed by the antennas.

Each of the passband signals is forwarded to block 2, where it is fed to an amplifier with 16 dB fixed gain. Specifically, we use an ADL5566 dual RF operational amplifier for each splitted

pair of passband signals. This amplifier has a low latency and a very flat frequency response, including a channel-to-channel gain and phase errors of 0.1 dB and 0.06°, respectively, at 100 MHz. Furthermore, the ADL5566 supports input signals with up to 4.5 GHz bandwidth without having the amplification vary over frequency, while hardly affecting the SNR due to its low noise input stage of only $1.3nV/\sqrt{Hz}$. Thus, the receiver contains four ADL5566 amplifiers for the four RF input signals. The wideband range property of ADL5566 makes our hardware suitable for a broad range of RF signals used in actual communication systems.

The signals from the amplifiers are separated into two groups. Each group has four inputs, including one signal from each splitted pair. Then, each signal is splitter again into two signals with 90° offset, which are used as the inputs to a phase shifter and gain block. The purpose of this additional splitting with phase offset stems from the fact that we use differential phase shifters, which operate on such inputs. In block 3, each of the four channels in one of the groups is activated by an ADL5390 analog vector multiplier, implementing the phase and gain of each analog combining weight applied to the input signal. The weights applied in the vector multiplications are determined by the output dc level of an AD7808 octal 10-bit DACs with serial load capabilities, which receives control commands from the FPGA board used to configure the analog combining weights by finding a look-up table. The usage of controllable gains and phases requires a calibration stage when the interconnections are established to guarantee that the configured weights are correctly translated into the desired phase and gain values.

Arguably, the most common analog combiner architecture is based on phase shifters [9], [16], [17]. In practice, applied phase shifters are digitally controlled with phase resolutions typically above 5°. This crude resolution may significantly degrade the system performance by inducing quantization errors. In our novel combiner prototype, we used vector multiplexer ADL5390 as an analog phase shifter controlled by the 10-bit DAC, allowing to realize combiner with controllable gains as well as providing the ability to reach an improved resolution of less than 1.5° in phase.

The outputs of each group are summed up in block 4, which finalizes the realization process of analog combining and obtains a combined passband signal. Then, the combined signals are down-converted in block 5 using a set of ADL5382 down-converters with the same local oscillator used for up-conversion. The down-converted signals are filtered to BB signals with a maximum 125 MHz bandwidth. Finally, the signals of the two outputs are forwarded to the FPGA where they are acquired using a 4DSP FMC168 16-bit digitizer card, obtaining the digital outputs for further digital signal processing in the computing center.

V. EXPERIMENT RESULTS

In the experimental study, we evaluate the channel estimation performance when the observed channel output is combined using our analog combining hardware, configured as both a CGAC as well as a PSOAC. While we focus here on MSE channel estimation, the proposed analog combiner can be used

to evaluate various other measures, such as bit error rate, by using different processing of the combined output, e.g., symbol detection, in the digital domain. We implement CGAC, designed via (10) by setting $\mathbf{V} = \mathbf{D} = \mathbf{I}_{N_{rf}}$, and PSOAC, configured using Algorithm 1. The channel estimation accuracy is compared to that achievable when using a random antenna selection, which randomly selects N_{rf} out of N_{bs} antennas, and also to the traditional fully digital setup, where each antenna is connected to a dedicated RF chain.

In all the presented experiments, the number of UT is fixed to $K = 3$, and the pilot sequence length is $\tau = K = 3$. Following [14], we fix the transmit side correlation matrix \mathbf{P} to the $K \times K$ identity matrix. The receive side correlation matrix \mathbf{Q} is generated as follows: for a fixed $N_Q > 0$, we randomize an $N_{bs} \times N_Q$ proper-complex Gaussian matrix with i.i.d. zero-mean unit variance entries, denoted $\tilde{\mathbf{Q}}$, and set $\mathbf{Q} = \tilde{\mathbf{Q}}\tilde{\mathbf{Q}}^*$. We consider two settings of N_Q : $N_{rf} < N_Q \leq N_{bs}$, referred to as the *regular setting*, and $N_Q = N_{rf}$, referred to as the *best setting*. We generate 1000 independent realizations of \mathbf{Q} . It is noted that the general clustered channel model [32], [33] is a special case of our Kronecker channel model used here [13]. The performance metric is the normalized MSE $\frac{\|\mathbf{h} - \hat{\mathbf{h}}\|^2}{\|\mathbf{h}\|^2}$ over the generated receiver correlation matrices. For each Monte Carlo simulation, new realizations of the channel matrix, noise vector, and pilots matrix are generated. Such noise vector and channel matrix obey the model detailed in Section IV. The pilots matrices are obtained from K eigenvectors of a $\tau \times \tau$ random matrix randomized from a proper-complex Gaussian distribution with i.i.d. zero-mean unit variance entries.

A. Normalized MSE Versus SNR

We first test the normalized MSE in estimating the channel versus SNR in the range [0, 30] dB, for an analog combiner with $N_{bs} =$ eight antennas and $N_{rf} =$ four RF chains. Note that this analog combiner model is obtained using the virtual channel extension approach detailed in Section IV. The results are depicted in Fig. 6(a)–(b) for high rank (regular) receive correlation and for low rank (best) receive correlation, respectively. Observing Fig. 6(a)–(b), we note that using the proposed hardware prototype, the PSOAC configured via Algorithm 1, which represents a practical family of analog combiners, achieves channel estimation accuracy within a very small gap compared to the costly CGAC architecture. Furthermore, both PSOAC and CGAC architectures notably outperform the random antenna selection approach. It is noted, however, that random antenna selection is simpler to implement compared to analog-combiner based systems, which require additional hardware. As expected, the fully digital architecture achieves the lowest MSE performance, as it has access to the observed channel output without dimensionality reduction.

For the high rank (regular) receiver correlation case, it is seen in Fig. 6(b) that all approaches, which implement analog combining, meet an error floor at high SNR (above 20 dB). This error floor is due to the model mismatch induced by the dimensionality reduction, which becomes the main performance bottleneck at this SNR regime. However, when the rank of the receive correlation matrix is not larger than the number of

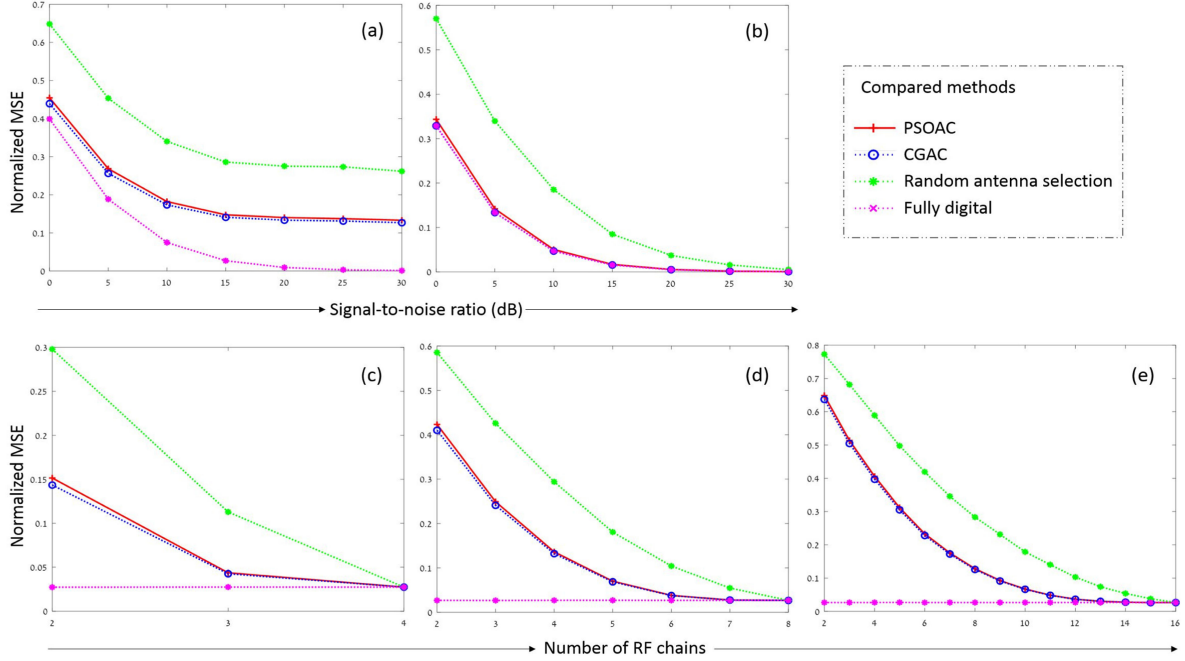


Fig. 6. Normalized MSE curves for analog combiners versus SNR with (a) the regular rank case and (b) the best rank case of the receive side correlation matrix. The normalized MSE curves at SNR of 15 dB and the regular rank case for the analog combiners with (c) 4 antennas, (d) 8 antennas, and (e) 16 antennas.

RF chains, the optimal MSE performance observed using fully digital receivers is also achievable using our analog combiner prototype, in line with the theoretical results of [13].

B. Normalized MSE Versus Number of RF Chains

Next, we numerically evaluate the normalized MSE performance achievable using our hardware analog combiner prototype for different numbers of RF chains. Here, we let the number of RF chains N_{rf} vary in the range of $[2, N_{bs}]$, for a fixed SNR level of 15 dB, and for a high rank (regular) receive correlation setup. The results of this experiment are depicted in Fig. 6(c), (d), and (e), for $N_{bs} = \{4, 8, 16\}$, respectively. Observing Figs. 6(c)–(e), we note that for all considered scenarios, the normalized MSEs of our hybrid architectures approach the normalized MSEs of the fully digital receiver as the number of RF chains increases. This result settles with the fact that for $N_{rf} = N_{bs}$ these networks implement a fully digital receiver. When the reduction rate $\frac{N_{rf}}{N_{bs}}$ is above 62.5%, the performance gaps between the proposed analog combiners and the fully digital receiver become negligible. This behavior is due to the numerical observation that most simulated channels can be reliably characterized by roughly 5/8 of their eigenmodes, which are reliably recovered and restored using our analog combiner hardware prototype. Moreover, among the hybrid receivers, the PSOAC achieves normalized MSE values, which are only slightly higher than that of the costly CGAC, emphasizing the benefits of its design via Algorithm 1. Finally, both the CGAC as well as the PSOAC have lower normalized MSEs than the random antenna selection.

These results demonstrate the ability of our proposed configurable analog combiner hardware to efficiently implement desirable RF chain reduction while inducing minimal performance degradation on the overall communication system.

VI. CONCLUSION

In this article, we presented a hardware prototype of a MIMO receiver with RF chain reduction via configurable analog combining. Our proposed prototype consists of a specially designed combiner board as well as a dedicated experimental setup, which allows to test and adjust the analog combiner weights. We configure the analog combiner to optimize the channel estimation accuracy in MIMO systems by proposing an algorithm, which improves upon state-of-the-art design methods. Using our hardware prototype, we were able to achieve MIMO channel estimation accuracy, which is comparable to that achievable using costly fully digital receivers.

APPENDIX PROOF OF THEOREM 1

Let $\mathbf{W} = \mathbf{V}\mathbf{\Lambda}\mathbf{U}^*$ be the singular value decomposition of \mathbf{W} , where $\mathbf{V} \in \mathbb{C}^{N_{rf} \times N_{rf}}$ and $\mathbf{U} \in \mathbb{C}^{N_{bs} \times N_{bs}}$ are its left and right singular matrices, respectively, and $\mathbf{\Lambda} \in \mathbb{C}^{N_{rf} \times N_{bs}}$ is its singular values diagonal matrix. To prove the theorem, we first note that the objective (7) is invariant to the choice of the unitary $\mathbf{V} \in \mathcal{U}$, and, thus

$$\begin{aligned} f(\mathbf{W}) &= f(\mathbf{\Lambda}\mathbf{U}^*) \\ &= \text{tr}((\mathbf{P} \otimes \mathbf{Q})(\mathbf{S}^* \otimes \mathbf{U}\mathbf{\Lambda}^*)) \\ &\quad \times [(\mathbf{S} \otimes \mathbf{\Lambda}\mathbf{U}^*)(\mathbf{P} \otimes \mathbf{Q}) + p_n \mathbf{I}_{K n_{bs}}](\mathbf{S}^* \otimes \mathbf{U}\mathbf{\Lambda}^*)^{-1} \\ &\quad \times (\mathbf{S} \otimes \mathbf{\Lambda}\mathbf{U}^*)(\mathbf{P} \otimes \mathbf{Q})^*. \end{aligned} \quad (15)$$

Next, we write $\mathbf{\Lambda}\mathbf{U}^* = \tilde{\mathbf{\Lambda}}\tilde{\mathbf{U}}^*$ where $\tilde{\mathbf{\Lambda}} \in \mathcal{D}$ and $\tilde{\mathbf{U}} \in \mathbb{C}^{N_{bs} \times N_{rf}}$ are the first N_{rf} columns of $\mathbf{\Lambda}$ and \mathbf{U} , respectively. Using this formulation, it is noted that (15) is invariant to the setting of $\tilde{\mathbf{\Lambda}}$,

and can be written as

$$\begin{aligned}
 f(\mathbf{W}) &= f(\tilde{\mathbf{U}}^*) \\
 &= \text{tr} \left((\mathbf{P} \otimes \mathbf{Q})(\mathbf{S}^* \otimes \tilde{\mathbf{U}}) \right. \\
 &\quad \times \left[(\mathbf{S} \otimes \tilde{\mathbf{U}}^*)((\mathbf{P} \otimes \mathbf{Q}) + p_n \mathbf{I}_{K n_{bs}})(\mathbf{S}^* \otimes \tilde{\mathbf{U}}) \right]^{-1} \\
 &\quad \times (\mathbf{S} \otimes \tilde{\mathbf{U}}^*)(\mathbf{P} \otimes \mathbf{Q})^* \Big) \\
 &\stackrel{(a)}{=} K \cdot \text{tr} \left(\tilde{\mathbf{U}}^* \alpha^2 \mathbf{Q}^2 \tilde{\mathbf{U}} \left[\tilde{\mathbf{U}}^* (\alpha \mathbf{Q} + p_n \mathbf{I}_{n_{bs}}) \tilde{\mathbf{U}} \right]^{-1} \right)
 \end{aligned} \tag{16}$$

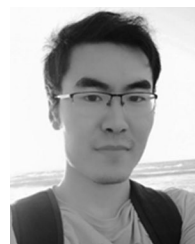
where (a) follows from the cyclic invariance property of the trace operator and by substituting $\mathbf{P} = \alpha \mathbf{I}_K$ and $\mathbf{S} \mathbf{S}^* = \mathbf{I}_\tau$. The optimization in (16) is then solved using $\tilde{\mathbf{U}} = \mathbf{U}^0$ by [13, Prop. 2], concluding the proof of the theorem. ■

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Tierui Gong (Student Member, IEEE) is currently working toward the Ph.D. degree with the University of Chinese Academy of Sciences, Beijing, China.

From 2018 to 2019, he was a Visiting Student with the Faculty of Mathematics and Computer Science, Weizmann Institute of Science, Rehovot, Israel, and was a Visiting Student with Faculty of Electrical Engineering, Technion—Israel Institute of Technology, Haifa, Israel. His research interests include cognitive radio, massive MIMO communications, and signal processing.



Nir Shlezinger (Member, IEEE) received the B.Sc., M.Sc., and Ph.D. degrees in 2011, 2013, and 2017, respectively, from Ben-Gurion University, Beersheba, Israel, all in electrical and computer engineering.

From 2017 to 2019, he was a Postdoctoral Researcher with the Technion, Israel Institute of Technology, and he is currently a Postdoctoral Researcher with the Signal Acquisition, Modeling, Processing and Learning Lab, Weizmann Institute of Science, Rehovot, Israel. From 2009 to 2013, he was a Research and Development Engineer with Yitran Communications.

His research interests include communications, information theory, signal processing, and machine learning.



Shahar Stein Ioushua (Student Member, IEEE) received the B.Sc. degree in electrical engineering (cum laude) in 2015 and the M.Sc. degree in electrical engineering (cum laude) in 2018, both from the Technion—Israel Institute of Technology, Haifa, Israel. She is currently working toward the Ph.D. degree in electrical engineering with Tel-Aviv University (TAU), Tel-Aviv, Israel.

From 2015 to 2020, she was a Teaching Assistance with the Viterbi Faculty of Electrical Engineering and the Iby and Aladar Fleischman Faculty of Engineering,

Tel Aviv University, and a Project Supervisor with the Signal Acquisition, Modeling and Processing Lab, at the Electrical Engineering Department, Technion. She is a Co-Founder of the WomEng forum of women in engineering with Tel Aviv university and the WomEE forum for women in graduate studies in the Electrical Engineering Department, Technion. Her research interests include information theory, data compression, theoretical aspects of signal processing, compressed sensing, and signal processing for communication signals.

Miss. Stein Ioushua received the Weinstein for excellent research and the Meyer Foundation Excellence prize, and is a Gutwirth Fellow since 2017.



Moshe Namer received the B.Sc. degree in electrical and communication engineering from Technion, the Israel Institute of Technology, Haifa, Israel, in 1984.

From 1984 to 2010, he was an Engineer with the Communication Lab, Electrical Engineering Department, Technion, leading analog and RF circuits student projects in hardware implementations. Since 2010, he has been active in SAMPL lab, headed by Yonina Eldar, working on hardware demo implementations.



Zhijia Yang received the B.Sc. degree from the College of Information Science and Electronic Engineering, Zhejiang University, Hangzhou, China, in 1990, and the Ph.D. degree in mechatronic engineering from the University of Chinese Academy of Sciences, Beijing, China, in 2012.

He is currently a Professor with the Shenyang Institute of Automation, Chinese Academy of Sciences, Shenyang, China, and was a Senior Visiting Scholar with the University of Sydney, Sydney, Australia. His research interests include industrial communications,

industrial Internet of Things, system on a chip, and embedded systems.

Dr. Yang was the Chief of the first domestic Foundation Fieldbus Communication Protocol Stack and Fieldbus Communication Controller chip. He once won the Second Prize of the National Scientific and Technological Progress Award twice in 2002 and 2009, respectively.



Yonina C. Eldar (Fellow, IEEE) received the B.Sc. degree in physics in 1995 and the B.Sc. degree in electrical engineering in 1996 both from Tel-Aviv University, Tel-Aviv, Israel, and the Ph.D. degree in electrical engineering and computer science in 2002 from the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA.

She is currently a Professor with the Department of Mathematics and Computer Science, Weizmann Institute of Science, Rehovot, Israel. She was previously a Professor with the Department of Electrical

Engineering, Technion, where she held the Edwards Chair in Engineering. She is also a Visiting Professor with MIT, a Visiting Scientist with the Broad Institute, and an Adjunct Professor with Duke University, Durham, NC, USA, and was a Visiting Professor with Stanford. Her research interests include the broad areas of statistical signal processing, sampling theory and compressed sensing, learning and optimization methods, and their applications to biology and optics.

Dr. Eldar has received many awards for excellence in research and teaching, including the IEEE Signal Processing Society Technical Achievement Award (2013), the IEEE/AESS Fred Nathanson Memorial Radar Award (2014), and the IEEE Kiyo Tomiyasu Award (2016). She is a Member of the Israel Academy of Sciences and Humanities (elected 2017) and a EURASIP Fellow. She was a Horev Fellow of the Leaders in Science and Technology program at the Technion and an Alon Fellow. She received the Michael Bruno Memorial Award from the Rothschild Foundation, the Weizmann Prize for Exact Sciences, the Wolf Foundation Krill Prize for Excellence in Scientific Research, the Henry Taub Prize for Excellence in Research (twice), the Hershel Rich Innovation Award (three times), the Award for Women with Distinguished Contributions, the Andre and Bella Meyer Lectureship, the Career Development Chair at the Technion, the Muriel and David Jacknow Award for Excellence in Teaching, and the Technions Award for Excellence in Teaching (two times). She received several best paper awards and best demo awards together with her research students and colleagues including the SIAM outstanding Paper Prize, the UFFC Outstanding Paper Award, the Signal Processing Society Best Paper Award, and the IET Circuits, Devices, and Systems Premium Award, and was selected as one of the 50 most influential women in Israel. She was a Member of the Young Israel Academy of Science and Humanities and the Israel Committee for Higher Education. She is the Editor-in-Chief of *Foundations and Trends in Signal Processing*, a Member of the IEEE Sensor Array and Multichannel Technical Committee and serves on several other IEEE committees. In the past, she was a Signal Processing Society Distinguished Lecturer, Member of the IEEE Signal Processing Theory and Methods and Bio Imaging Signal Processing technical committees, and served as an Associate Editor for the IEEE TRANSACTIONS ON SIGNAL PROCESSING, the *EURASIP Journal of Signal Processing*, the *SIAM Journal on Matrix Analysis and Applications*, and the *SIAM Journal on Imaging Sciences*. She was Co-Chair and Technical Co-Chair of several international conferences and workshops.